

OPTIMIZATION OF COPPER VIA FILLING PROCESS FOR FLEXIBLE PRINTED CIRCUIT USING RESPONSE SURFACE METHODOLOGY

K.Y. Wong¹, P.J. Liew¹, K.T. Lau² and J. Wang³

¹Faculty of Manufacturing Engineering,
Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian
Tunggal, Melaka, Malaysia.

²Faculty of Mechanical and Manufacturing Engineering Technology,
Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian
Tunggal, Melaka, Malaysia.

³Marine Engineering College,
Dalian Maritime University, 1 Linghai Road, Ganjingzi District, Dalian 116026,
China.

Corresponding Author's Email: 1payjun@utem.edu.my

Article History: Received 20 May 2020; Revised 13 June 2020;
Accepted 23 August 2020

ABSTRACT: Copper filling is a method for 3D stacked packaging and has been widely used in the semiconductor industry. However, as the downsizing of devices becomes an unavoidable trend, the tolerance of flexible printed circuit (FPC) fabrication has to decrease, resulting in high failure rates. To solve this problem, optimal process variables for copper filling must be studied to avoid the risk of failure. In this study, the effects of copper via filling parameters (current density (I_a), fluid flow rate (Q) and filling time (t_f)) on the filling behavior of a micro via (surface thickness, dimple depth and via filling ratio) were investigated. The via on the FPC board was drilled using a laser drill with a dimension of 100 μm . Then, the FPC was immersed in an electrolyte for the copper via filling process. Experimental results showed that current density was significant to surface thickness, whereas fluid flow rate was significant to the dimple depth and via filling ratio. The optimum parameters to achieve thin surface thickness, low dimple depth and high via filling ratio were found to be at 1.5 A/dm² of current density, 35 m³/h of fluid flow rate and 60 min of filling time.

KEYWORDS: *Copper Via Filling; Flexible Printed Circuit; RSM Optimization*

1.0 INTRODUCTION

Copper filling is a method for 3D stacked packaging to deposit copper in a bottom-up or superfilling mode for ensuring void-less filling in a copper via. It has many advantages, such as avoidance of short circuits, reduction of current leakage and prevention of electromigration. This method remains the most promising 3D packaging technology because it can enhance the performance of flexible printed circuit (FPC) with a small form factor, low weight, high current flow rate, low power consumption and good electrical performance by interconnecting chips with the shortest vertical path [1].

During the copper filling process, if the parameters used are not optimal, the copper filled micro via will undergo overplating or underplating [2]. This situation leads to the formation of seams, dimples and bumps on the micro via [3]. In the previous study, Yen et al. [4] investigated the effects of solution flow and current density on the filling behavior of copper-filled micro via. They discover low levels of solution flow and current density improved filling performance. Wang et al. [5] studied the effects of via depth on current density and filling patterns. They claimed that the deeper the via is, the lower the optimum current density is. They also argued that when a low I_d is applied, the filling patterns do not change as the via depth changes.

Although extensive researches have been performed on the effect of filling parameters, however, there is no study has focused on the optimization of current density, fluid flow rate and filling time on the filling behavior of copper-filled micro vias. Therefore, in this study, the effects of copper via filling parameters (current density (I_d), fluid flow rate (Q) and filling time (t_f)) on the filling behavior of a copper filled micro via (surface thickness, dimple depth and via filling ratio) were investigated. The optimal parameters for the copper via filling process were determined and validated at the end of this study.

2.0 EXPERIMENTAL METHODS

2.1 Materials and Equipment

An industrial copper via filling machine was used to perform the experiment. A multilayer FPC with a thickness of 244 μm was selected as the specimen material. The electrolyte system utilized to perform the copper via filling process was manufactured by Atotech Malaysia Sdn. Bhd. Figure 1 provides a schematic of the copper via filling process.

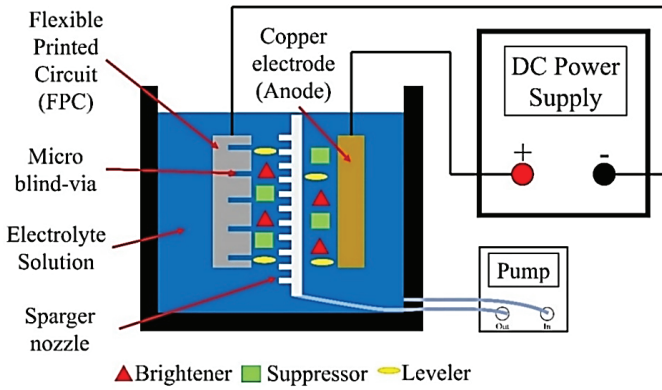


Figure 1: Schematic of the copper via filling process

2.2 Experimental Design

The Box–Behnken design response surface methodology (BBD-RSM) was used to analyze the correlation between the parameter and the experiment result [6]. Three controllable parameters, I_d , Q and t_f , were considered. In this analysis, two levels of parameters were designed (Table 1), and the proposed values (low and high) for the levels were selected based on industry specifications. The matrix contained 39 runs and included three replications. The outputs were surface thickness (μm), dimple depth (μm) and via filling ratio (%). The confidence levels of all the models were set to 95%. Therefore, all insignificant terms ($P\text{-value} > 0.05$) were removed using the model reduction technique.

Table 1: Factors and levels

Parameters	Low	High
Current density, I_d (A/dm^2)	1	2
Fluid flow rate, Q (m^3/h)	15	35
Filling time, t_f (min)	60	120

2.3 Measurement and Analysis

After the filling process, the filled via was cut out from the FPC, and the cross section of the filled via was fabricated using acrylic resin and polished by using a surface grinding and polishing machine. The surface thickness, dimple depth and area of the via were observed under a Keyence VK-X200 series high-power laser microscope with a magnification of $50\times$ and $100\times$. The via filling ratio was calculated using Equation (1) [7].

$$\text{Via Filling Ratio} = \frac{\text{Area of Via} - \text{Area of Void}}{\text{Area of Via}} \times 100\% \quad (1)$$

The data were recorded and inserted into the RSM matrix that generated by Minitab software to determine the relationship of the parameters with via properties. Figure 2 illustrates the via cross-sectional microstructure.

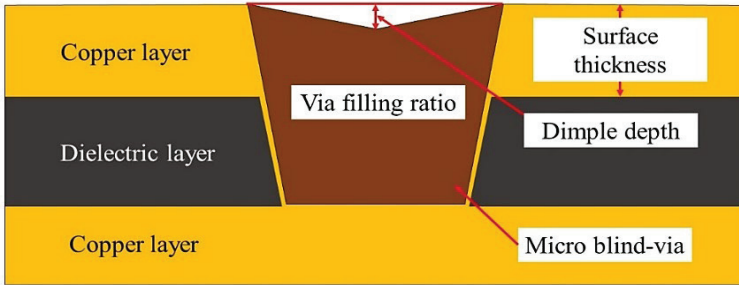


Figure 2: Illustration of the via cross section

3.0 RESULTS AND DISCUSSION

3.1 Surface Thickness

Table 2 presents the ANOVA for surface thickness. The significance level of the terms can be determined by monitoring the P-value, which is smaller than 0.05. In this case, all factors are considered significant to the model; therefore, model reduction can be neglected. The lack of fit has a P-value > 0.05 (such as 0.45) which can be classified as insignificant in this model. This means that the data of the result fit with the model. The mathematical model for value prediction is shown in Equation (2).

Table 2: ANOVA table of surface thickness

Source	DF	Adj SS	Adj MS	F-Value	P-Value	Correlation
Model	9	1072.01	119.112	72.22	0.000	Significant
Linear	3	954.29	318.096	192.88	0.000	Significant
I_d (A/dm ²)	1	608.51	608.507	368.97	0.000	Significant
Q (m ³ /h)	1	162.77	162.77	98.7	0.000	Significant
t_r (min)	1	183.01	183.01	110.97	0.000	Significant
Square	3	30.39	10.129	6.14	0.002	Significant
$I_d \times I_d$	1	16.45	16.449	9.97	0.004	Significant
$Q \times Q$	1	24.51	24.507	14.86	0.001	Significant
$t_r \times t_r$	1	13.57	13.565	8.23	0.008	Significant
Two-way Interaction	3	87.34	29.112	17.65	0.000	Significant
$I_d \times Q$	1	42.43	42.432	25.73	0.000	Significant
$I_d \times t_r$	1	25.09	25.095	15.22	0.001	Significant
$Q \times t_r$	1	19.81	19.811	12.01	0.002	Significant
Error	29	47.83	1.649			
Lack of fit	3	4.54	1.515	0.91	0.450	
Pure error	26	43.28	1.665			
Total	38	1119.84				

$$\begin{aligned}
 \text{Surface} &= -22.0 + 29.38I_d + 1.384Q + 0.122t_f \\
 \text{thickness} &= -6.20(I_d)^2 - 0.01891(Q)^2 - 0.001563(t_f)^2 \\
 (\mu\text{m}) &= -0.3761(I_d \times Q) + 0.0964(I_d \times t_f) + 0.00428(Q \times t_f)
 \end{aligned} \tag{2}$$

Figure 3 shows the plot of the main effects of I_d , Q and t_f on the surface thickness of FPC. The surface thickness presented logarithmic growth along with increasing I_d , Q and t_f , but only Q showed a trend of decrease at the end of the graph. Amongst all the parameters, I_d has the most significant effect on surface thickness, as evidenced by its inclination line being greater than those of Q and t_f .

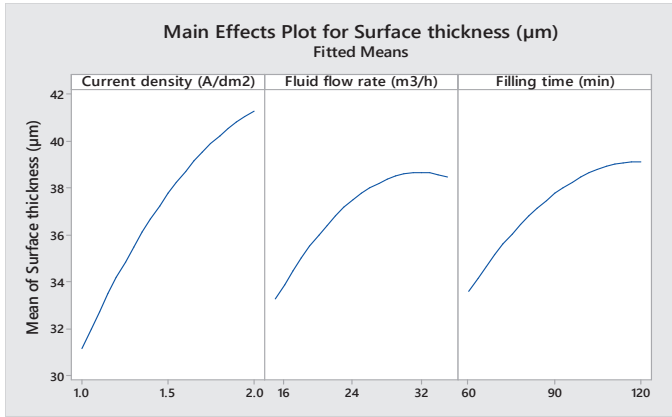


Figure 3: Plot of the main effects on surface thickness

This phenomenon can be explained from the viewpoint of deposition rate. As I_d increased, the deposition rate also increased. When t_f remained constant, a high deposition rate resulted in a substantial amount of copper deposited on the surface and thus increased the surface thickness of FPC. This result is supported by Zhu et al. [8] who found that a higher I_d leads to the rapid growth of copper deposition, especially at the opening of microvia.

Similarly, when I_d and Q were fixed, the growth of t_f may cause more charges were supplied to the cathode (FPC surface). The cathode then exposed to a substantial amount of copper ion during the deposition process and causing the thickness of FPC surface increased. This finding matches with the study by Wang et al. [1]. They found that throughout the filling duration of 30 min, 60 min, 90 min, 150 min and 300 min, more copper was deposited on the surface as the time increases.

Unlike I_d and t_f , Q showed an increasing trend initially and decreasing afterward. This phenomenon was due to the enhanced mass exchange

of electrolyte bring more copper ions come into contact with the cathode when the Q increases, which speed up the copper deposited on the surface and thicken the surface thickness. However, if the Q exceeds its optimal, the excessive Q will create a vortex that limits the mass exchange of electrolyte and causing a reduction in deposition rate. These results are in agreement with those obtained by Engelmaier and Kessler [9] who highlighted that over or lesser than optimum level of Q will lead to the decrease of deposition rate.

3.2 Dimple Depth

After the analysis of ANOVA for dimple depth, only the ‘Linear’ terms, ‘ $t_f \times t_f$ ’ and ‘ $I_d \times t_f$ ’ were significant to the result (P-value smaller than 0.05). As the ‘Lack of fit’ term was also significant to the model, therefore the insignificant terms must be removed through the model reduction technique in order to reduce the high error occurrence probability of the model.

Table 3 was created after model reduction and the P-value of ‘Lack of fit’ is increased to 0.0620, which indicates that the ‘Lack of fit’ for this model is not significant anymore and the data of the result is now fit to the model. The mathematical model used for value prediction is shown in Equation (3).

Table 3: ANOVA table for dimple depth

Source	DF	Adj SS	Adj MS	F-Value	P-Value	Correlation
Model	5	30258.9	6051.8	445.26	0.0000	Significant
Linear	3	29835	9945	731.7	0.0000	Significant
I_d (A/dm ²)	1	3500.6	3500.6	257.56	0.0000	Significant
Q (m ³ /h)	1	24647.7	24647.7	1813.46	0.0000	Significant
t_f (min)	1	1686.6	1686.6	124.09	0.0000	Significant
Square	1	252.6	252.6	18.59	0.0000	Significant
$t_f \times t_f$	1	252.6	252.6	18.59	0.0000	Significant
Two-way interaction	1	171.3	171.3	12.6	0.0010	Significant
$I_d \times t_f$	1	171.3	171.3	12.6	0.0010	Significant
Error	33	448.5	13.6			
Lack of fit	7	169.6	24.2	2.26	0.0620	
Pure error	26	278.9	10.7			
Total	38	30707.4				

$$\text{Dimple depth } (\mu\text{m}) = 109.8 - 1.49I_d - 3.2047Q + 1.145t_f - 0.00581(t_f)^2 - 0.2519(I_d \times t_f) \tag{3}$$

Figure 4 illustrates the main effects plot for the dimple depth of the via. Based on Figure 4, Q is the most significant effect as it is the one with the highest inclination to the responses, followed by I_d and t_f .

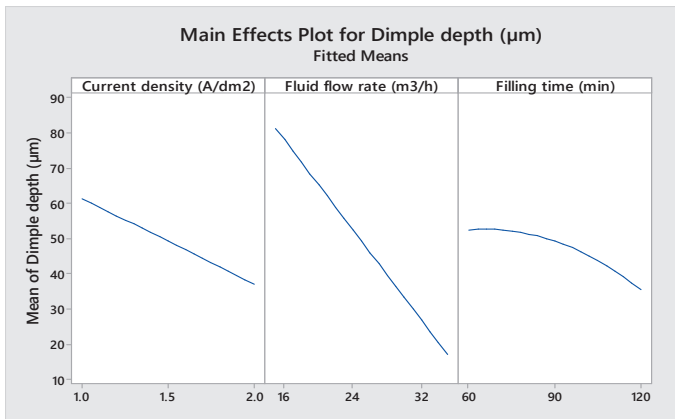


Figure 4: Plot of the main effects on dimple depth

Figure 4 indicates that dimple depth decreases with an increase in I_d . When I_d increased, the high copper deposition rate caused the opening of the via closed before the via was fully filled, and resulting in the formation of a void or inclusion even though the dimple was shallow. This finding is consistent with the study of Pan et al. [10] and Wang et al. [11]. The situation can be explained by Figures 5(a) and 5(b) which show the cross-sectional image of two vias that were filled at the same Q and t_f but different I_d . The via filled with a higher I_d (Figure 5a) presented a void and shallower dimple while the via with lower I_d (Figure 5b) shows a deeper dimple but lack of void.

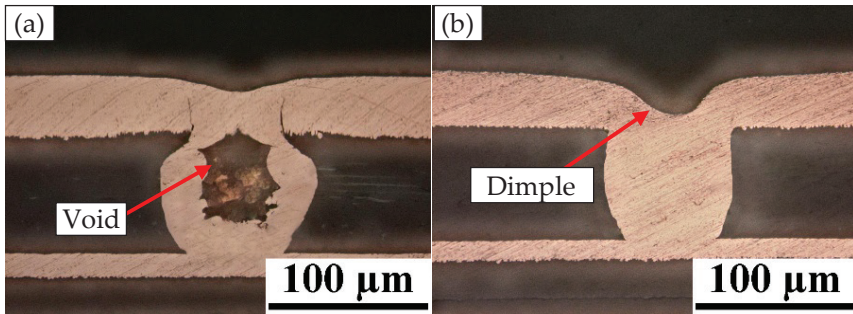


Figure 5: Cross section of (a) void-filled ($I_d = 2A$, $Q = 35 \text{ m}^3/\text{h}$, $t_f = 90 \text{ min}$) and (b) dimpled ($I_d = 1A$, $Q = 35 \text{ m}^3/\text{h}$, $t_f = 90 \text{ min}$) micro vias

In addition, Q showed a linearly inverse proportion to the dimple depth. The mass exchange of copper ions in the dimple also became high at high value of Q . When the dimple was exposed to substantial copper ions, the copper was easy to be deposited and filled into the dimple, and this causing a lower dimple depth. This explanation is further supported by Nikolova et al. [12] who stated that a higher Q is recommended to achieve a quality via fill without defects.

Next, t_f also presented a decreasing trend with dimple depth. When t_f was longer, there are more charges were supplied to FPC. As a result, the excessive amount of charge will attract copper ion and deposited in the via and causing the dimple depth decreased [13].

3.3 Via Filling Ratio

Table 4 provides the ANOVA for via filling ratio. All of the terms are significant to the model, therefore the model reduction is not needed in this case. On the other hand, the P-value for 'Lack of fit' of the model was 0.083, and it shows that the model fits the data of via filling ratio. The mathematical model used for value prediction is shown in Equation (4).

Table 4: ANOVA table for via filling ratio

Source	DF	Adj SS	Adj MS	F-Value	P-Value	Correlation
Model	9	11719.3	1302.15	467.52	0.000	Significant
Linear	3	7931.7	2643.91	949.27	0.000	Significant
I_d (A/dm ²)	1	392.5	392.47	140.91	0.000	Significant
Q (m ³ /h)	1	6573	6573.01	2359.98	0.000	Significant
t_f (min)	1	966.3	966.26	346.93	0.000	Significant
Square	3	3656.6	1218.86	437.62	0.000	Significant
$I_d \times I_d$	1	2662.2	2662.15	955.82	0.000	Significant
Q \times Q	1	28.8	28.82	10.35	0.003	Significant
$t_f \times t_f$	1	44.8	44.82	16.09	0.000	Significant
Two-way interaction	3	131	43.68	15.68	0.000	Significant
$I_d \times Q$	1	23	23.04	8.27	0.007	Significant
$I_d \times t_f$	1	94.1	94.12	33.79	0.000	Significant
Q \times t_f	1	13.9	13.89	4.99	0.033	Significant
Error	29	80.8	2.79			
Lack of fit	3	18	6.01	2.49	0.083	
Pure error	26	62.7	2.41			
Total	38	11800.1				

$$\begin{aligned} \text{Via filling ratio (\%)} = & 118.6 + 204.62I_d - 0.109Q + 0.353t_f \\ & -78.81(I_d)^2 + 0.02050(Q)^2 - 0.002841(t_f)^2 \\ & +0.2771(I_d \times Q) + 0.1867(I_d \times t_f) + 0.00359(Q \times t_f) \end{aligned} \quad (4)$$

Figure 6 presents the plot of the main effects on via filling ratio. In the figure, the via filling ratio increased with Q and t_f . Q was more significant than t_f because the via filling ratio raised exponentially with Q and only growth logarithmically with t_f . On the contrary, the via filling ratio increased with rising I_d but eventually changed to decreasing trend after the optimum point.

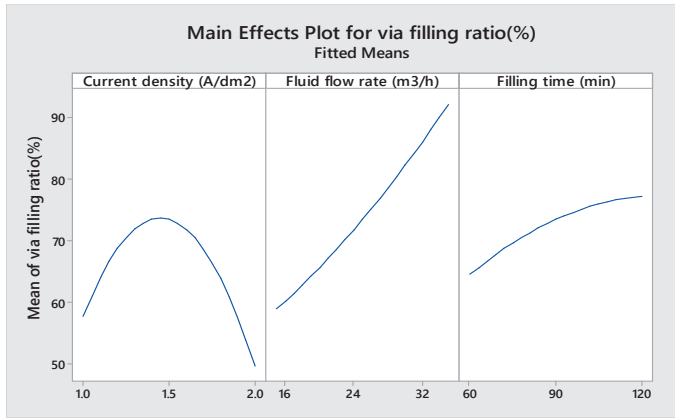


Figure 6: Plot of the main effects on via filling ratio

As presented in Figure 6, the via filling ratio increased when Q increased. This is because an increment in Q enhances the mass exchange of copper ions. This situation causes the via to be exposed to abundant copper ions, which enlarges the via filling ratio. This result is in line with the finding of Nagai et al. [14] who observed a rise in via filling ratio as the filling time increase.

Moreover, when t_f was longer, the number of charge supplied and the time frame of the via exposed to the copper ion were also higher. It stimulates the deposition process and increases the amount of copper deposited in the via. Therefore, if I_d and Q remain constant, a copper via with a longer t_f will tend to have a higher via filling ratio. This result is supported by Wang et al. [15] and Wang et al. [1] where they confirmed that when t_f increase leads to the rise of via filling ratio.

With regard to I_d , a possible explanation for this might be the boosted deposition rate that caused by the increase of I_d . When I_d is overly high, the higher copper deposition rate exceed the bottom-up growth rate, where the opening of via come to contact and merge together. When the opening was closed, there is no electrolyte mass exchange occurred inside the via, this leads to the failure of superfilling, void inside and decreases the via filling ratio. These results are similar to those reported by Wang et al. [1] who claimed that when I_d passed through the optimum point, the via filling ratio declined because of an excessively high deposition rate and causing the opening of the copper via closed before the via bottom part is completely filled.

3.4 Optimization of the Process Parameters

Table 5 provides the optimization goals and lower and upper limits for each response. The industry standard indicates that a quality-filled via must have a thin surface, a small dimple depth, and a high via filling ratio. Therefore, the goal for each response was to achieve defectless copper via filling. The optimum values selected through the software for each parameter and the corresponding response value optimized in accordance with the goal are shown in Table 6.

Table 5: Optimization goal for optimum parameters

Response	Goal	Lower limit	Upper limit
Surface thickness (µm)	Minimum	23.6491	44.2455
Dimple depth (µm)	Minimum	4.503	99.6137
Via filling ratio (%)	Maximum	34.3213	96.7399

Table 6: Summary of the optimization plot

Parameter	Optimum value	Response	Optimum result
Current density (A/dm ²)	1.5	Surface thickness (µm)	32.4399
Fluid flow rate (m ³ /h)	35	Dimple depth (µm)	22.7191
Filling time (min)	60	Via filling ratio (%)	82.1446
		Composite desirability	0.708103

Table 6 shows that the optimized parameters are $I_d = 1.5 \text{ A/dm}^2$, $Q = 35 \text{ m}^3/\text{h}$ and $t_f = 60 \text{ min}$. Their corresponding optimized responses are via filling ratio of 82.145%, dimple depth of 22.72 µm and surface thickness of 32.44 µm. This combination owns a composite desirability of 0.7081.

3.5 Validation Test

After the prediction of the optimum values, a validation test was performed to validate the accuracy of the analyzed results. A set of random parameters that were not included in the DoE matrix was selected for the validation test. The predicted results of the chosen random parameters were obtained through Minitab software. Afterward, the random parameters were applied to the validation test, in which three replications of each result were recorded. Table 7 shows the random parameters, predicted results and validated results.

Table 7: Results of the validation test

Random parameters = $I_d = 1.5 \text{ A/dm}^2$, $Q = 25 \text{ m}^3/\text{h}$, $t_f = 60 \text{ min}$						
Responses	Predicted result	Experimental replication			Average	Error (%)
		1	2	3		
Surface thickness (µm)	33.592 µm	32.798	34.512	35.688	34.333	2.205%
Dimple depth (µm)	52.5 µm	56.868	53.113	53.694	54.558	3.921%
Via filling ratio (%)	64.598 %	62.982	63.875	62.031	62.963	2.531%

As presented, the error percentage of the validated results was 2.205% for surface thickness, 3.921% for dimple depth and 2.531% for via filling ratio. This outcome indicates that the predicted result is close to the validated result, given that the confidence level of this study is 95% and all errors do not exceed 5%. Thus, the optimization of filling parameters to maximize the quality of the filled via was validated.

4.0 CONCLUSION

This study provides a basic fundamental understanding of the relation between copper via filling parameters (I_d , t_f and Q) and the filling behavior of copper filled micro vias (surface thickness, dimple depth and via filling ratio). The optimum parameters were determined through Minitab software with the application of RSM. The following main conclusions were derived.

- i. I_d , t_f and Q are crucial in controlling the filled via properties.
- ii. The via filling ratio improves as Q and t_f increase, but only a suitable optimal I_d (1.5 A/dm²) produces the optimum result.
- iii. I_d and t_f strongly affect the surface thickness of FPC during the process. Higher I_d and t_f result a higher surface thickness.
- iv. Q increases with surface thickness, but the slope of the increment trend decreases as Q increases.
- v. t_f , I_d and Q decrease with dimple depth. The higher t_f , I_d and Q are, the lower the dimple depth is.
- vi. The optimum parameters ($I_d = 1.5$ A/dm², $Q = 35$ m³/h and $t_f = 60$ min) produce a surface thickness of 32.44 μ m, dimple depth of 22.71 μ m and via filling ratio of 82.14%.
- vii. The composite desirability of the optimized result is 0.708103.

ACKNOWLEDGEMENTS

The authors are grateful to Universiti Teknikal Malaysia Melaka (UTeM) and MFS Technology (M) Sdn. Bhd. for providing the equipment and materials used in this research.

REFERENCES

- [1] F. Wang, X. Ren, P. Zeng, H. Xiao, Y. Wang and W. Zhu, "Dynamics of filling process of through silicon via under the ultrasonic agitation on the electroplating solution," *Microelectronic Engineering*, vol. 180, pp. 25–29, 2017.
- [2] M. Schlesinger and M. Paunovic, *Modern Electroplating, 5th Edition*. New Jersey: John Wiley and Sons, 2010.
- [3] H. Huebner, R.S. Mertens and D. Ruess, "Copper filling of blind micro vias and through holes using reverse pulse plating," *PCB Magazine 007*, vol. 4, no. 5, pp. 24–34, 2014.
- [4] M.Y. Yen, M.H. Chiang, H.H. Tai, H.C. Chen, K.W. Yee, C. Li, M. Lefebvre and M. Bayes, "Next generation electroplating technology for high planarity, minimum surface deposition microvia filling," in *International Microsystems, Packaging, Assembly and Circuits Technology Conference*, Taiwan, 2012, pp. 259–262.
- [5] F. Wang, Z. Zhao, N. Nie, F. Wang and W. Zhu, "Effect of via depth on the TSV filling process for different current densities," *Journal of Micromechanics and Microengineering*, vol. 28, no. 4, pp. 1–11, 2018.
- [6] A.B. Hadzley, W.M. Azahar, A.A. Anis, R. Izamshah, M. Amran, S. Kasim and S. Noorazizi, "Development of surface roughness prediction model using response surface methodology for end milling of HTCS-150," *Journal of Advanced Manufacturing Technology*, vol. 12, no. 1, pp. 467–476, 2018.
- [7] F. Wang, W. Liu and Y. Wang, "Effects of additives with different acids on the through-silicon vias copper filling," *Microelectronic Engineering*, vol. 200, pp. 51–55, 2018.
- [8] Y. Zhu, W. Luo, Z. Chen, M. Li and L. Gao, "Influence of electroplating current density on through silicon via filling," in *International Conference on Electronic Packaging Technology*, China, 2015, pp. 153–157.
- [9] W. Engelmaier and T. Kessler, "Investigation of agitation effects on electroplated copper in multilayer board plated-through holes in a forced-flow plating cell," *Journal of The Electrochemical Society*, vol. 125, no. 1, pp. 36–43, 1978.
- [10] H. Pan, Y. Zhang, M. Li and L. Gao, "Effect of pretreatment on copper filling of high aspect ratio through-silicon via (TSV)," in *International Conference on Electronic Packaging Technology*, China, 2018, pp. 672–675.
- [11] F. Wang, Z. Zhao, F. Wang, Y. Wang and N. Nie, "A novel model for through-silicon via (TSV) filling process simulation considering three additives and current density effect," *Journal of Micromechanics and Microengineering*, vol. 27, no. 12, pp. 1–12, 2017.

- [12] M. Nikolova, C. Rodriguez, K. Feng, C. Gugliotti, W. Bowerman, J. Watkowski and B. Wei, "Via fill and through hole plating process with enhanced TH microdistribution," *PCB Magazine 007*, vol. 8, no. 11, pp. 78–90, 2018.
- [13] W.P. Dow, M.Y. Yen, S.Z. Liao, Y.D. Chiu and H.C. Huang, "Filling mechanism in microvia metallization by copper electroplating," *Electrochimica Acta*, vol. 53, no. 28, pp. 8228–8237, 2008.
- [14] M. Nagai, Y. Tamari, N. Saito, F. Kuriyama, A. Fukunaga, A. Owatari, S. Masashi and C. Moore, "Electroplating copper filling for 3D packaging," in *Electronic Components and Technology Conference, USA, 2009*, pp. 648–653.
- [15] J. Wang, M. Wu and C. Cui, "Factors governing filling of blind via and through hole in electroplating," *Circuit World*, vol. 40, no. 3, pp. 92–102, 2014.

