IMPACT OF TaN/Ta BILAYER ON THE BULK RESISTIVITY OF COPPER LAYER AT VARIOUS SELF-ANNEALING TIME

M.N. Abd Rahman[1], A.F. Ahmad[2], Z.S. Hashim[1], M.R. Muhamad[1], and E. Budi[3]

[1]Fakulti Kejuruteraan Pembuatan,
Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.

[2]Department of Thin Film Metal, Diffusion and Implant,
Silterra Malaysia Sdn. Bhd.,
Kulim Hi-Tech Park,
09600 Kulim, Kedah, Malaysia.

[3]Faculty of Mathematics and Science,
Universitas Negeri Jakarta, Jl. Rawamangun Muka,
Jakarta Timur, 13220 Indonesia.

Corresponding Author's Email: [1]mdnizam@utem.edu.my

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ABSTRACT: Copper layer metallization in back-end-of line interconnect is widely adopted in integrated circuit manufacturing. One of the issues faced in most of integrated circuit manufacturing industry is the restriction of 12 hours maximum delay time between the copper seed deposition and copper electroplating step. This is due to claim of possible sheet resistance (Rs) instability as a result of copper diffusion into silicon even though with the presence of TaN/Ta bilayer barrier between silicon dioxide layer and copper layer. There is lack of study and data to justify support this time restriction or on the effectiveness of the TaN/Ta bilayer barrier in stabilizing sheet resistance of copper layer as a function of self-annealing time. This study evaluates the effectiveness of Ta/TaN barrier to prevent changes in Rs of copper seed layer as a function of self-annealing time. The result indicates that the The TaN/Ta bilayer barrier improve the stability of Rs of the copper seed layer at various level of self-annealing time. However, the t-test analysis shows that at 95% confidence level, statistically there is significant drop in Rs for both experimental lots (with and without TaN/Ta bilayer barrier) comparing the 0 hour and 12 or 36 hours of self-annealing time.

KEYWORDS: *Integrated Circuit Manufacturing; Self-Annealing; Copper Seed; Physical Vapor Deposition*

1.0 INTRODUCTION

The trend in integrated circuit (IC) manufacturing is towards, small form factor, high performance and low cost. This is the basic requirements for survival in current electronic products market. One of the important aspects in IC fabrication is the back-end-of-line (BEOL) interconnect. The BEOL interconnect is IC fabrication process that connects the individual devices, such as transistors, capacitors, and resistors. Materials to be used for the BEOL interconnect must have low resistivity, high electromigration reliability, low diffusivity, and of course low cost [1-2]. This is the main reason copper (Cu) is predominantly selected as the BEOL interconnect materials over Ag, Au, or Al. The low resistance of Cu enables significant shrinkage in critical dimensions without sacrificing device speed [3].

One of the concerns in Cu as the BEOL interconnect materials is lack of self-limiting oxide layer to impede the diffusion of Cu into silicon (Si) and its affinity to diffuse into Si even at low annealing temperature [4-5]. Due to that, diffusion barrier is common between Si and Cu layer to minimize inter-diffusion of Cu atoms or ions and also other neutral molecules. The common barrier used in IC industries is Ta/TaN layer. The additional barrier layer tends to increase resistivity of the interconnect system. Due to that, minimization of the barrier layer thickness is usually pursued to minimize its effect on resistance-capacitance (RC) value [6].

Typical Cu metallization process consists of two main stages. Initial step is Cu seeding process where a thin layer of Cu is deposited using Physical Vapor Deposition (PVD). Subsequent to that, bulk Cu layer is deposited on top of the Cu seed using Electroplating process (ECP). Most IC manufacturing facility, imposes maximum delay time of 12 hours between Cu seeding and ECP process. The reasoning for this restriction is the claim by IC tool manufacturer that Cu sheet resistance (Rs) will degrade as a function of staging time. There are some related studies related to the effect room temperature aging, or self-annealing, on properties of Cu layer. It was reported that self-annealing contributed to the increase in grain size and change in film stress [5-6]. One related study is by Huang et al. [7] who investigated the sheet resistance, stress, and microstructure of self-annealed copper layer post electroplating process. Most of the reported studies investigated the effect of the self-annealing time post Cu ECP process [8-9]. However, there is lack of study done on the effect of self-annealing time post Cu seeding process or the effect of Ta/TaN bilayer barrier on the Rs as a function of self-annealing time. The aim of this study is to assess the effectiveness of

Ta/TaN barrier to prevent changes in Rs of Cu seed layer as a function of self-annealing time.

2.0 EXPERIMENTAL PROCEDURE

2.1 Deposition Process

Wafer used in this study is 200mm polished Silicon wafer with crystallographic orientation of (100). The evaluated categorical factors are ageing period and application of Ta/TaN bilayer barrier. The experimental lots consist of two different stackings, with and without Ta/TaN bilayer barriers. The two stackings are as shown in Figure 1.

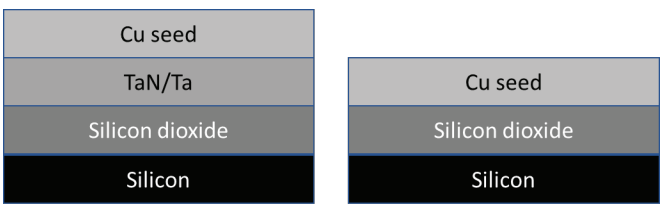

Figure 1: Experimental device stacking: (a) with TaN/Ta bilayer and (b) without TaN/Ta bilayer

The synthesis of stack-up layer and the experimental flow is as the process flow shown in Figure 2. Prior to Cu seeding process, 2 nm thick silicon dioxide is grown on silicon wafer, or also called substrate, using tetraethyl orthosilicate (TEOS) as the precursor. After the synthesis of silicon oxide layer, for experimental lot with barrier layer, Ta/TaN bilayer is deposited in the Applied Materials Endura P5500 Barrier Seed PVD deposition cluster tool. This tool consists of an outgassing chamber, a Cu Oxide reduction chamber and a deposition chambers. The initial step of the synthetization process is the thermal outgassing of substrate to remove any moisture. Deposition of 30nm TaN/Ta bi-layer is done in the Ta high density plasma supported by radio frequency (RF) excitation and direct current (DC) biasing. TaN is formed by poisoning the Ta target material with the reaction gas, nitrogen (N_2). The Ta film is synthesized subsequently, in the same of reaction gas, N_2. The substrates for the experimental run without the TaN/Ta barrier are directly moved to Cu seeding deposition chamber after the synthetization of silicon oxide layer.

The Cu seed deposition chamber is in the same Endura Barrier Seed deposition PVD system with Self Ionized Plasma (SIP) deposition

capability. The sputtering occurs by means of self-sustaining ion bombardment onto the copper target. The substrate is subjected to voltage during the deposition of 120nm Cu seed film. All the substrates are processed in the same tool without vacuum break where the chambers are maintained at low pressure of 5E-8 Torr to minimize any inclusion of impurity in the deposition layer.

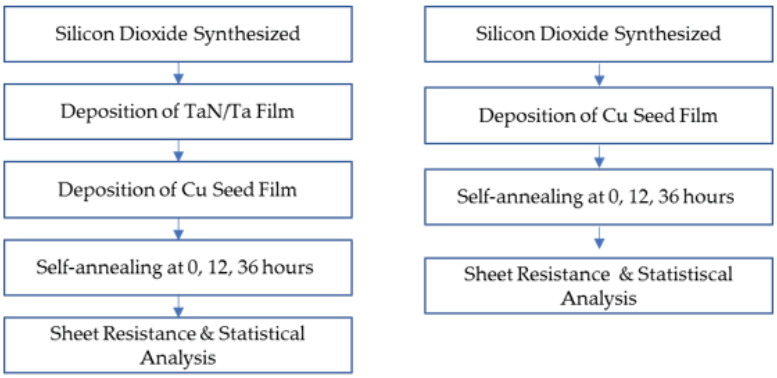

Figure 2 : Experimental lot process flow: (a) with TaN/Ta and (b) without TaN/Ta

2.2 Self-Annealing

The experimental lots for both device with and without TaN/Ta layer were then split into 3 lots. Each lot consisted of five specimens. The lots were self-annealed at 0, 12, and 36 hours before sent for sheet resistance, reflectance, and stress analysis as reflected in Figure 2. The selection self-annealing times of 0 hour is as a control, the 12 hours is the current maximum staging time set in production, and 36 hours is to evaluate if staging time can be extended to give flexibility to manufacturing operation. During the self-annealing process, the experimental lots were stored in standard wafer pods under class 100 mini clean-room environment.

2.3 Sheet Resistance and Statistical Analysis

The Cu film Rs of each experimental lot was measured using OmniMap Rs-100 with 1.6 mil tip type A four-point probe. In this method, the four metal tips were mechanically pressed on to the Cu layer surface to form a square and a current was passed through the outer tips. Based on the voltage measured and current value setting, the sheet resistance was calculated [10]. Statistical analysis in determining the significant differences between various experimental lots was carried out based on t-test analysis. The analysis utilizes Minitab software.

3.0 RESULTS AND DISCUSSION

3.1 Bulk Resistivity for Cu Seed Without and With TaN/Ta Bilayer Barrier

The scatter plot shown in Figure 3 depicts the bulk resistivity trend for Cu seed without and with TaN/Ta bilayer after seed without ECP. Stack that without TaN/Ta bilayer barrier, bulk resistivity drops rapidly for the first 12 hours and more gradually only after 24 hours. However, only small rate of reduction is seen for stack with TaN/Ta bilayer barrier seed ageing in the first 12 hours. In perspective, during the first 12 hours, the bulk resistivity reduction rates are at 4.965 nΩ-m per hour for without TaN/Ta bilayer and 0.578 nΩ-m per hour on the with TaN/Ta bilayer. Stack without TaN/Ta bilayer has almost 10 times greater rate of reduction compare to stack with TaN/Ta bilayer. After 24 hours ageing, bulk resistivity reduction rates for stack without and with TaN/Ta bilayer are at 0.005 nΩ-m and 0.001 nΩ-m, respectively.

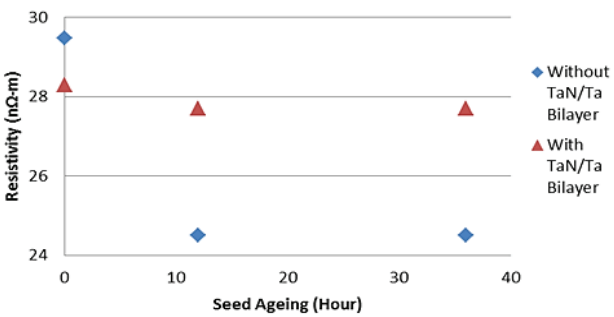

Figure 3: Resistivity trend of Cu seed after self annealing

These phenomenon matches with the observation from previous study where that TaN/Ta bilayer barrier has the capability to stabilize the sheet resistance by blocking Cu and SiO_2 inter-diffusion [11]. Further study is needed to understand the underlying mechanism at work in bulk resistivity stabilizing property with the inclusion of bilayer film. Other studies show that properties Cu and Ta can be changed by modulating ion bombardment and substrate bias during deposition [9,12-13]. Perhaps with this knowledge, better bilayer property can be engineered and a more robust Cu stack sheet resistance achievable. This is imperative if current restriction of 12 hours maximum waiting time between copper seeding and copper electroplating process are to be extended.

3.2 Statistical Analysis on Copper Seed Layer Rs Data for Experimental Lots Without and With TaN/Ta Bilayer Barrier

In order to analyze the statistical significance of this finding, a t-test analysis was carried out. The box plot of bulk Rs for the stack without TaN/Ta bilayer barrier are plotted in Figure 4 and the summary of the t-test analysis is tabulated in Table 1.

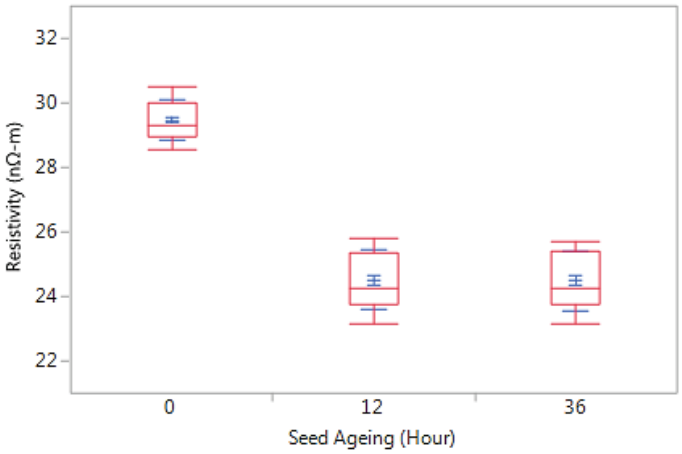

Figure 4: The box plot of bulk Rs for the stack without TaN/Ta bilayer barrier

within the same range of that of 36 hours self-annealing Rs data. This observation is supported by the t-test summary in Table 1. The prob > t value for 12 hours and 0 and 36 hours and 0 are less than 0.05, indicating statistically there are significant difference in Rs value between those data. The prob > t value for 12 hours and 36 hours comparison of 0.9761 indicates that statistically the values of Rs between those self-annealing time are not different. Moreover, Figure 5 shows the box plot of bulk Rs for the stack with TaN/Ta bilayer barrier and the summary of the t-test analysis is tabulated in Table 2.

Table 1: T-test summary of the Rs without TaN/Ta layer

Comparing Pair	**12 with 0**	**36 with 0**	**36 with 12**
Difference	-4.9655	-4.9706	-0.00508
Std Err Dif	0.1695	0.1695	0.16946
Upper CL Dif	-4.6306	-4.6357	0.32987
Lower CL Dif	-5.3005	-5.3056	-0.34003
Confidence	0.95	0.95	0.95
t Ratio	-29.3021	-29.3321	-0.02999
DF	144	144	144
Prob >|t|	<.0001*	<.0001*	0.9761

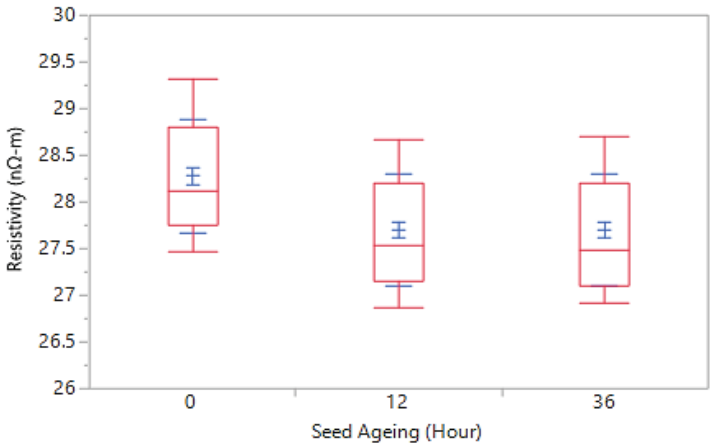

Figure 5: The box plot of bulk Rs for the stack TaN/Ta bilayer barrier

Visually, the box-plot in Figure 5 indicates Rs data for the 0 hour self -annealing is in the closer range compare to Rs data for the 12 and 36 hours of self-annealing compared to the observation on the box plot for Rs data without the TaN/Ta bilayer. However, based on the t-test summary in Table 2, the Prob > t for comparison between 0 and 12 hours and 0 and 36 hours are less than 0.05. Based on this, statistically the Rs for 0 hour self-annealing are significantly different that that of 12 hours and 36 hours self-annealing time. This indicates that even though the TaN/Ta bilayer barrier improve the Rs stability as indicated in trend chart in Figure 3, there is still significant reduction is Rs for experimental lot with TaN/Ta bilayer.

The boxplot of Rs data for the 12 hours and 36 hours self-annealing in Figure 5 indicates they are within the same range and this is supported by the t-test summary in Table 2; the prob > t value for 12 hours and 36 hours comparison is 0.9933, indicating statistically there is no significant difference in Rs value between those data.

Table 2: T-test summary of the Rs with TaN/Ta layer

Comparing Pair	**12 with 0**	**36 with 0**	**36 with 12**
Difference	-0.57839	-0.57941	-0.00102
Std Err Dif	0.12109	0.12109	0.12109
Upper CL Dif	-0.33904	-0.34006	0.23833
Lower CL Dif	-0.81774	-0.81876	-0.24037
Confidence	0.95	0.95	0.95
t Ratio	-4.77635	-4.78478	-0.00843
DF	144	144	144
Prob >|t|	<.0001*	<.0001*	0.9933

4.0 CONCLUSION

The result indicates that the The TaN/Ta bilayer barrier improve the stability of Rs of the copper seed layer at various level of self-annealing time. However, the t-test analysis shows that at 95% confidence level, statistically there is significant drop in Rs for both experimental lots (with and without TaN/Ta bilayer barrier) comparing the 0 hour and 12 or 36 hours of self-annealing time Rs data. Based on these data, further optimization of the TaN/Ta deposition process is recommended to improve its function is stabilizing Rs property of the copper seed film.

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