FIXED-POLE ACTIVE PI FILTER DESIGN FOR HIGH FREQUENCY NONLINEAR PLL MODELS

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ABSTRACT: A Phase-locked loop (PLL) is a basic control system that attempts to produce an output waveform that can match with the input reference signal in the shortest time possible. A filter is one of the main components in the PLL blocks, and it plays a very important role to determine the range of input frequency that can ensure the system stays in a locked condition. This paper focuses on designing a fixed-pole active PI filter which is suitable for high-frequency PLL-based circuits such as those used in clock generators. As PLL is bound to fall out of lock due to the nonlinear effects from its phase detector, a new approach is introduced in this work which is to combine the linear and nonlinear control method to ensure stability. Having had the phase margin specified a priori, it is shown by simulation that the allowable range of input frequency such that the system remains locked can be expanded.

KEYWORDS: *Nonlinear PLL; Active PI Filter; Phase Margin*

1.0 INTRODUCTION

The basic function of a PLL system is to ensure that the phase and frequency of the output signal are equivalent to those of the input signal. The PLL system is fundamental to many electronic circuits used for frequency control such as clock synchronization and distribution [1]. It is also commonly used in a telecommunication system for modulation/demodulation and frequency synthesizer [2-3]. With the technology advancement in the electronic system, advanced development of the PLL circuit was successfully implemented on a single integrated chip (IC) back in the year 1965 [4]. Since then, the demand for this type of IC design with higher performance captures the attention of many researchers [5-6]. The PLLs have also been used for high-frequency application [7-9] which include clock generators for microprocessors of which the operation frequencies start at 100MHz and above [10].

The PLL structure usually consists of a phase detector (PD), loop filter (LF), and voltage controlled oscillator (VCO) [11]. Each of these blocks has an important role to ensure the system functions accurately according to the desired specifications. The performance of the PLL system which is usually indicated by the locking range and settling time also depends on the parameters of the filter [12]. Three basic filter types mostly used in PLL design are passive, active and proportional integral (PI) filters. Another important parameter that can be considered in the filter design is phase margin. Few studies which discuss the impact of the phase margin on loop response can be found in [13-15].

As most PLL systems are nonlinear due to the effects from the PD and VCO [16–19], extensive studies regarding their stability and working frequency range have been carried out since the past few decades [20–23]. These include classical graphical techniques [20], LaSalle theorem [21] and Lyapunov redesign [22]. For nonlinearities that can be categorized as sector- and slope-bounded, the circle and Popov criteria can provide sufficient stability conditions for the closed-loop systems under certain assumptions [23].

In this paper, an alternative method is proposed to design a fixed-pole second order active PI filter for nonlinear PLL by combining linear and nonlinear design approaches. In this new method, we use the H_∞ control technique where the phase margin is specified a priori. The performance of the nonlinear PLL system in terms of locking range and locking time is then compared with the filter designed when the phase margin is allowed to take any values.

2.0 METHODOLOGY

Assuming all high frequency components have been attenuated, the resulting block diagram of PLL in phase domain can be illustrated in Figure 1.

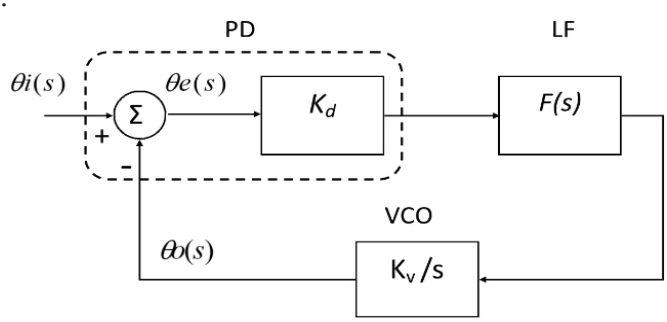


Figure 1: General block diagram for a linear PLL model in phase domain [24]

The transfer function of the closed-loop PLL without considering nonlinearity can be written as:

$$G(s) = \frac{K_d K_v F(s)}{s + K_d K_v F(s)} \tag{1}$$

where the K_d and K_v is the PD gain (volts/rad) and VCO gain (rad/volt second) respectively. Whereas F(s) is the filter's transfer function which takes the form:

$$F(s) = \frac{K_0 s^2 + K_1 s + K_2}{s^2} \tag{2}$$

which is also known as fixed-pole active PI filter. To ensure the stability of the PLL system in the linear region, sufficient gain or phase margins must be preserved. The phase margin $\emptyset_m$ (in degree) can be determined by the parameter γ as follows [25]:

$$\left|\frac{H(s)}{1 + H(s)}\right| < \gamma \tag{3}$$

where H(s) is the open loop transfer function of the PLL system. The useful relationship between phase margin $\emptyset_m$ and γ can be approximated by the following equation:

$$\gamma \approx \frac{1}{2\sin(0.5\emptyset_m)} \tag{4}$$

The closed-loop system in Figure 1 can be restructured into Figure 2, with the state space system P written as:

$$\begin{aligned} \dot{x} &= A_a x + B_1 w + B_2 u \\ z &= C_1 x \\ y &= C_2 x \end{aligned} \tag{5}$$

and the state space of the filter given by:

$$u = K_L x \tag{6}$$

with notation that $\boldsymbol{C} = [\boldsymbol{C_1} \quad \boldsymbol{C_2}]^{\boldsymbol{T}} = [\boldsymbol{1} \quad \boldsymbol{0}]^{\boldsymbol{T}}$ and $\boldsymbol{z} = \boldsymbol{u}$.

The resulting closed-loop system becomes:

$$M \sim \begin{bmatrix} A_a + B_2 K_L & B_1 \\ K_L & 0 \end{bmatrix} \tag{7}$$

which is suitable for $\boldsymbol{H}_\infty$ synthesis framework.

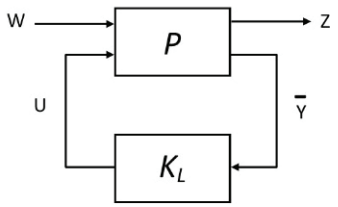


Figure 2: General block diagram for H_∞ synthesis

The following method can then be applied:

Lemma 1: H_∞ approach [25].
Given an LTI system $\widetilde{M}(s) = C(sI - A)^{-1}B + D$. Then the following statements are equivalent:

i. A is Hurwitz stable and $\left\|\widetilde{M}(s)\right\|_\infty < \gamma$.
ii. There exists a positive definite matrix $P = P^T$ such that the following LMI hold.

$$\begin{bmatrix} A^T P + PA & PB_1 & C^T \\ {B_1}^T P & -\gamma I & D^T \\ C & D & -\gamma I \end{bmatrix} \leq 0 \tag{8}$$

In order to ensure stability of the PLL when it is subjected to the nonlinear effect from the PD, the nonlinear function needs to be included as shown in Figure 3. It is then straightforward to rearrange the loop into the so-called Lur'e system [26] which is suitable for application of the circle criterion. Assuming the nonlinearity $\emptyset$(y) is static, memoryless, and it satisfies the sector bounded as described by:

$$0 \leq \frac{\emptyset(y)}{y} \leq K, \quad \forall y \neq 0 \tag{9}$$

The following criterion can be applied:

Lemma 2: Circle Criterion [27].
Consider the system in Figure 3 and define $\widetilde{M} = K_d K_v F(s)/s = C(sI - A)^{-1}B + D$, and $\emptyset$ satisfying the sector given by Equation (8). The closed-loop system is absolutely stable if A is Hurwitz and the $\widetilde{M}(s)$ lies on the right-half plane of the Nyquist plot defined of $Re[s] = -1/K$ such as

$$Re\left[1 + K\widetilde{M}(j\omega)\right] > 0, \quad \forall \omega \in \mathbb{R} \tag{10}$$

By using Kalman-Yakubovich-Popov (KYP) Lemma [28], the frequency domain from the Equation (10) can be transformed into an LMI form given by:

$$\begin{bmatrix} A^T P + PA & PB - C^T \\ B^T P - C & -2\widetilde{K}^{-1} \end{bmatrix} \leq 0 \tag{11}$$

By integrating Lemmas 1 and 2, the proposal of a method to design the filter as follows:

Proposed method: Consider the fixed-pole an active PI filter as in Equation (2) and let K_I=[K_0 K_1 K_2]. Given γ>0, if Equations (12)-(14) are feasible,

$$\boldsymbol{X} > 0, \tag{12}$$

$$\begin{bmatrix} \boldsymbol{X}{A_a}^T + \boldsymbol{W}^T {B_2}^T + A_a \boldsymbol{X} + B_2 \boldsymbol{W} & B_1 - \boldsymbol{W}^T \\ {B_1}^T - \boldsymbol{W} & -2\widetilde{K}^{-1} \end{bmatrix} \leq 0, \tag{13}$$

$$\begin{bmatrix} \boldsymbol{X}{A_a}^T + \boldsymbol{W}^T {B_2}^T + A_a \boldsymbol{X} + B_2 \boldsymbol{W} & B_1 & \boldsymbol{W}^T \\ {B_1}^T & -\gamma I & 0 \\ \boldsymbol{W} & 0 & -\gamma I \end{bmatrix} \leq 0 \tag{14}$$

then the filter can be obtained by $K_L = WX^{-1}$.

Proof: Perform congruence transformation by pre- and post-multiplying of inequality Equation (13) by T=diag(X^{-1},I), and Equation (14) by T=diag(X^{-1},I,I), where X=P^{-1}, with a change of variable W=K_IX, Equations (10) and (11) is obtained respectively.

Remark 1: Without specifying γ a priori, an optimal filter may be obtained if Equations (12)-(14) are feasible by minimizing the parameter. In this case, we denote the method as method 1 for comparisons in the simulation results section.

3.0 SIMULATION RESULTS

The simulation of nonlinear PLL system is analyzed in phase domain model as shown in Figure 3. The nonlinearities from the PD can be characterized by a sine-wave or a triangular-wave such as

$$\emptyset(.) = \sin(\theta_e) \tag{15}$$

for the sine-wave; and for the triangular-wave [29].

$$\emptyset(.) = \frac{4}{\pi}\sum_{n=0}^{5}\frac{(-1)^n}{(2n+1)^2}\sin[(2n+1)\theta_e] \tag{16}$$

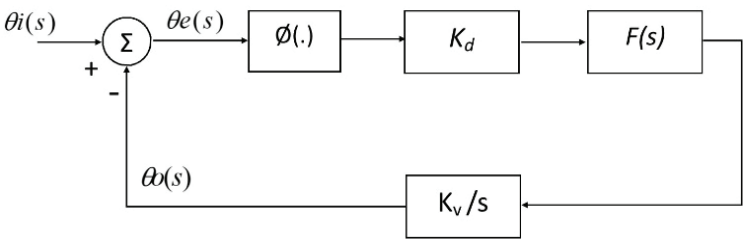


Figure 3: Nonlinear PLL system in phase domain

By setting the VCO gain, K_v=1, and PD gain, K_d=1, the parameters of the second order active PI filter obtained by using proposed method are given in Table 1. The results are compared with the designed filter via method 1.

Table 1: Second order filters' structure

Method	Filter, F(s)
Proposed Method	$\frac{4.088\times10^{10}s^2+1.444\times10^{8}s+2.924\times10^{5}}{s^2}$
Method 1	$\frac{2.689\times10^{8}s^2+3.639\times10^{6}s+3.133\times10^{4}}{s^2}$

Figure 4 shows the bode plot for linear PLL with designed filter via the proposed method and method 1. The plotted graph shows the closed-loop response of the PLL system at phase margin of 60^0, which γ equivalent to one.

The simulation results for step response (1Hz, 400MHz, and 500MHz) of the nonlinear PLL system with the designed filter via the proposed method and method 1 are shown in Figure 5. From the figure, at low input frequency of 1Hz, the step response for designed filter via the proposed method produced small overshoot. However, when the frequency was higher, no overshoot was observed. When the frequency was increased to 500MHz, it showed that the designed filter via method 1 failed to track the input, while the designed filter via the proposed

method remained locked. From the same graph, it can be easily seen that the steady state response for the designed filter via proposed method is much faster than method 1.

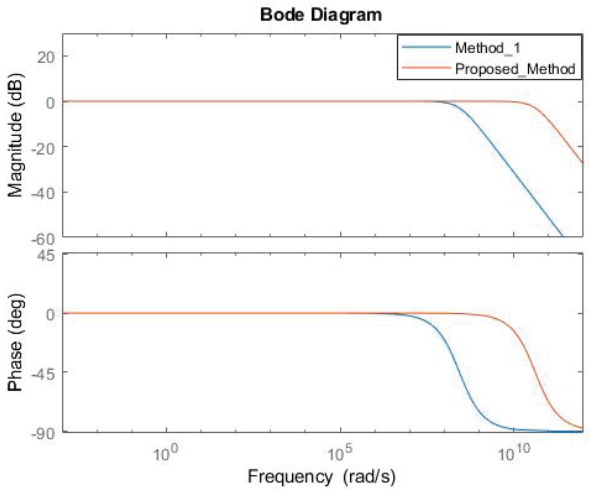
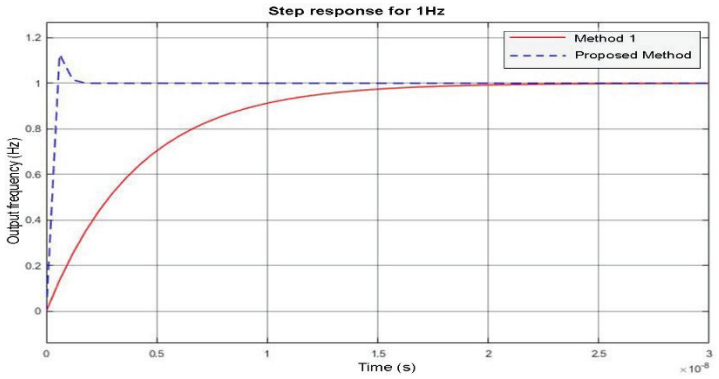


Figure 4: Bode plot for closed-loop linear PLL system with designed filter via the proposed method and method 1

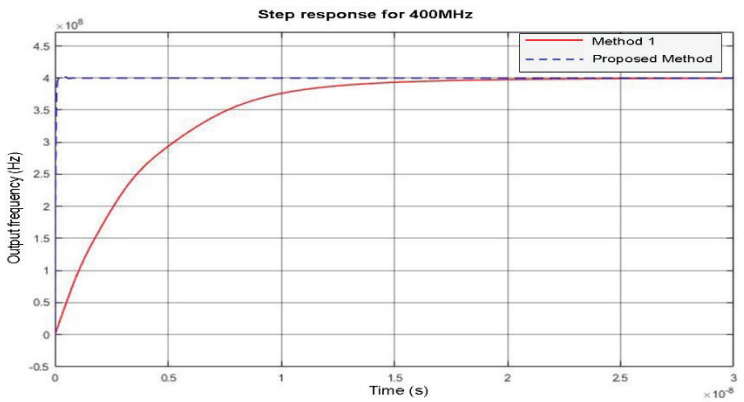
The locking range and settling time for the designed filter via the proposed method and method 1 are summarized in Table 2. The results are also compared with the nonlinearity from the sine-wave and triangular-wave PD. From the tabulated table, the locking range for the PLL system with the designed filter via the proposed method for both types of nonlinearities is larger than method 1. However, the settling times for both the designed filter via the proposed method and method 1 with sine-wave PD are much faster than the triangular-wave PD.

Table 2: The locking range(ω_L) and settling time (t_s) for nonlinear PLL system using triangular and sine-wave PDs for the proposed method and method 1

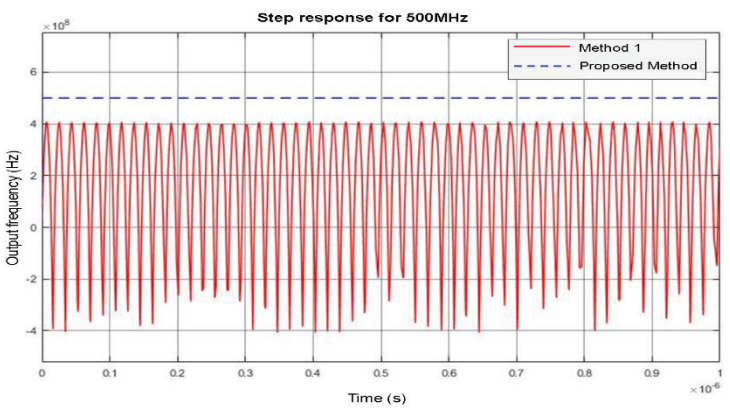
Performance	Sine-wave PD		Triangular-wave PD	
	ω_L(MHz)	t_s(s)	ω_L(MHz)	t_s(s)
Proposed method	40000	0.6 X 10^{-8}	60000	1.2 X 10^{-8}
Method 1	200	3.0 X 10^{-8}	400	3.8 X 10^{-8}



(a)



(b)



(c)

Figure 5: Step response for nonlinear PLL system with designed filter via proposed method and method 1 at frequencies (a) 1Hz, (b) 400MHz and (c) 500MHz using triangular-wave PD

4.0 CONCLUSION

In this paper, a new technique to design a fixed-pole active PI filter for nonlinear PLL system is presented. Based on the simulation results, the designed filter via the proposed method offers more advantages in terms of locking range and settling time as compared to method 1. This type of filter design is suitable for clock generator on electronic board application, which requires a frequency range of 100MHz and beyond. For future work, other values of phase margins can be considered to satisfy the PLL design for other types of applications with different performance specifications.

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