COPPER LAYER SHEET RESISTANCE EVOLUTION AS A FUNCTION OF POST-SEED PROCESS SELF-ANNEALING TIME

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ABSTRACT: Copper layer metallization is one of the important processes in integrated circuit manufacturing. One of the issues faced in this process is the proneness of Cu interface diffusion as well as surface oxidation which degrade some of the Cu thin film properties. Due to this concern, most integrated circuit manufacturing facility imposed 12 hours maximum delay time between the Cu seed deposition and Cu electroplating step. However, there is lack of study and data to justify support this time restriction. This study investigated the effect of self-annealing time between Cu seeding process and Cu electroplating process to the sheet resistance, reflectance, and stress of the deposited film. The data indicated that the there is no significant deterioration or fluctuation in sheet resistance, reflectance, and stress beyond 12 hours delay time. This suggested that the imposed 12 hours maximum delay time between Cu seed and Cu electroplating process can be further extended, which will give greater flexibility for the manufacturing scheduling.

KEYWORDS: Sheet Resistance; Post-Seed; Self-Annealing; Copper Film

1.0 INTRODUCTION

Copper is extensively used in Integrated Circuit (IC) manufacturing due to its low-cost, low-temperature processing requirement, and low resistivity characteristic [1]. Copper metallization low resistivity property, twice lower than that of aluminum, has been a key enabler to the shrinking of critical dimensions in today IC technology [2-3]. It greatly improves the resistor-capacitor circuit (RC) time-delay, critical in smaller geometry and higher performance devices today. However, this advantage comes at a price. Due to its high number of movable electron, copper is prone to element diffusivity and strong surface oxidation tendency [4].

A typical copper metallization process in IC manufacturing consists of two main process steps. The first step is called Cu seeding process where a thin layer of Cu is deposited using Physical Vapor Deposition (PVD). Subsequent to that, a bulk Cu layer is deposited on top of the Cu seed using Electroplating process (ECP). Most of IC manufacturing facility, based on the recommendation from tool suppliers, imposes maximum delay time of 12 hours between these two steps. The reasoning given by tool manufacturer for this delay time is the degradation of Cu sheet resistance (Rs) degrades as a function of time. The degradation of Cu Rs during exposure at room temperature, known as self-annealing, post-ECP has been attributed to the recrystallization of Cu layer. Some other reported microstructure changes related to self-annealing were the increase in grain size and change in film stress [5-6]. One related study by Huang et al. [7] investigated the sheet resistance, stress, and microstructure of self-annealed copper layer post electroplating process. However, this study did not investigate the effect of the self-annealing time post Cu seeding process.

A review of related literature indicates there is lack of study published to validate the necessity of imposing 12 hours maximum transient time between the Cu seeding and Cu ECP process. In addressing this gap, the aim of this study is to look into the variation of Cu seed resistivity as a function of delay times between Cu seeding and Cu ECP process. In addition to that reflectance data of the deposited Cu were also collected.

2.0 EXPERIMENTAL PROCEDURE

All Cu films samples were synthesized on 200 mm wafers with the crystallographic orientation of (100) per process flow is shown in Figure 1. Prior to physical vapor deposition process (PVD) of TaN/Ta and Cu seed, 2kÅ thick silicon dioxide was grown, using tetraethyl orthosilicate (TEOS) as the precursor, on the silicon wafer. Subsequently, a 200Å film of TaN/Ta bi-layer was then deposited as adhesion and barrier layers using PVD process.

A 1kÅ Cu seed layer was then deposited in a self-ionized plasma PVD chamber. The experimental samples were then split into seven lots and self-annealed at 0.5, 1, 2, 4, 6, 12, and 36 hours before sent for ECP process for copper layer deposition. During self-annealing process, the experimental lots were stored in standard wafer pods under class 100 mini clean-room environment. Figure 2 shows the wafer stacking for this study.

The Cu film Rs of each experimental lot was measured using OmniMap Rs-100 with 1.6 mil tip type A four-point probe. In this method, the four metal tips were mechanically pressed on to the Cu layer surface to form a square and a current was passed through the outer tips. Based on the voltage measured and current value setting, the sheet resistance was calculated.

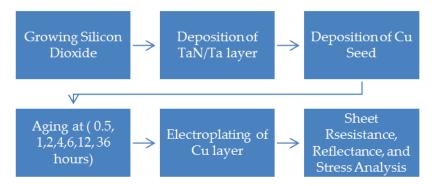


Figure 1: Sample preparation and sample analysis

ECP
Cu
TaN/Ta
SiO ₂
Si

Figure 2: Stacked diagram of prepared sample

The reflectance of copper films was analyzed using dual beam spectrometer, ASET-F5x thin film metrology system, to indicate the presence of grain boundary. The Rs and reflectance measurement were done as soon as the ECP was completed. Statistical analysis of the data was done using Minitab software version 18 to ascertain the statistical significance of the different experimental lots' data.

3.0 RESULT AND DISCUSSION

The interval plot of copper film sheet resistance for various post-seed self-annealing time is shown in Figure 3. In general, the trend indicates that there is a significant reduction in Rs for the first six hours from 212 ohm/sq to 207 ohm/sq. Rs reading for self-annealing time plateaus within the range of 207 ohm/sq to 206 ohm/sq beyond six hours self-annealing time. This suggested that the post Cu seeding self-annealing influenced the Rs of the Cu layer after EPC process. However, this influence diminished as the self-annealing time was extended beyond six hours.

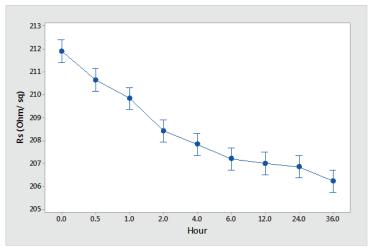


Figure 3: Interval plot showing the significant reduction in Rs up to 6 hours of self-annealing time

To ascertain this claim statistically, one-way analysis of variance (ANOVA) was carried out on the Rs data using Minitab software. The significance level for the ANOVA analysis was set at 0.05. Table 1 shows the summary of one-way ANOVA result with a p-value of 0.000. Since the p-value is less than the significant level of 0.05, statistically there, there is 0.0 % chance that the influence of post-seed self-annealing time on the Rs of the copper layer is due to chance. The Rs of the thin film is influenced mainly by the concentration of free

electron and electron mobility. The change in resistivity of Cu film as a function of post-seed self-annealing in this study can be attributed to the change in electron mobility. The electron mobility is mainly affected by lattice scattering, grain boundary scattering, and lattice scattering. These electrons scattering mechanisms are affected by defects in the Cu film such as grain boundaries, dislocation, and impurities [8]. The initial drop in Rs as shown in Figure 3 is believed to be as a result of the initial high rate of recrystallization due to high dislocation density during the post-seed self-annealing stage. During the initial stage of self-annealing, the rate of grain growth was high resulted in a reduction in grain boundary defect, hence, increasing the electron mobility and decreasing the Rs value.

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Source	DF	Adj SS	Adj MS	F-Value	P-Value
Hour	8	273.66	34.2080	63.42	0.000
Error	72	38.84	0.5394		
Total	80	312.50			

Table 1: One -way ANOVA for Rs by self-annealing time

The diminishing effect of self-annealing time was statistically analyzed using the mean comparison chart of one-way ANOVA using Minitab Software shown in Figure 4. It confirms that the mean of Rs for the post-seed self-annealing time of six hours and beyond are statistically the same.

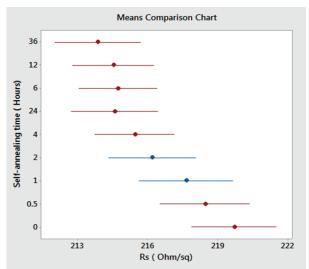


Figure 4: Mean comparison chart showing the stabilization of Rs value

This indicates that the prolong of waiting time between Cu seed process and Cu electroplating process beyond six hours will not significantly alter the Rs of the Cu layer. As mentioned earlier, the initial drop in Rs is attributed to the initial high rate of recrystallization due to high dislocation density [9]. During self-annealing, grain growth resulted in a reduction in the grain boundary and hence reduction in defect and drop in Rs. The rate of grain growth is mainly influenced by annealing time and temperature. Since the self-annealing temperature is fixed at room temperature, the rate of grain growth stabilized after a certain period of time [10]. This explained the stabilization of Rs beyond six hours of self-annealing time as reflected in Figure 3.

Figure 5 shows the linear prediction plot of regression analysis for Rs vs Reflection Index of the Cu layer. It suggests a positive relationship between the two with a coefficient of determination (R-squared) of 30.34%, suggesting some correlation between the two variables. However, the calculated probability value (P-value) of the linear regression model is less than 0.005; indicating a statistically significant positive correlation between Rs and reflectance index.

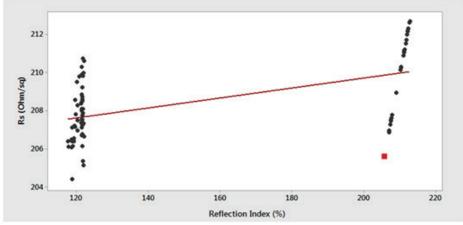


Figure 5: Regression for Rs vs reflection index

Reflectance index can indicate the amount of grain boundary of a Cu layer is the reflectance index. The higher the grain boundary, the lower the reflectance index is because grain boundary causes scattering. Due to that, the higher the reflectance index is the lower the grain boundary and the higher the grain surface [11]. Since grain boundary is considered a defect in Cu film that influences sheet resistance, there should be a negative correlation between reflectivity and sheet resistivity. However, Figure 5 shows a positive correlation between the two. This can be explained based on a study done by Brunoldi et al. [12] and Lagrange et al. [13], that suggested the optical reflectivity index was influenced mainly by surface chemical contamination rather than the grain size or grain boundary if there was chemical contamination present on the surface of Cu film.

The linear prediction plot of regression analysis for Rs vs Stress of the Cu layer is shown in Figure 6. It suggests an inverse relationship between the two with a coefficient of determination (R-squared) of 4.58%, suggesting a weak correlation between the two variables. However, the calculated probability value (P-value) of the linear regression model is less than 0.031 which is lower than the significance level of 0.05, indicating a significant correlation between Rs and stress. The previous study on the effect of self-annealing on Cu film suggested that grain growth during the self-annealing resulted in a continuous relaxation of Cu film stress [8, 14].

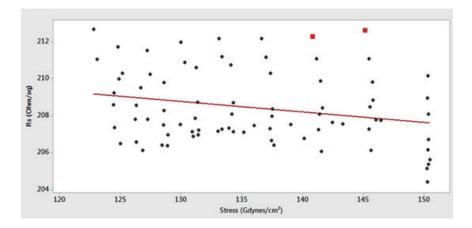


Figure 6: Regression for Rs vs stress

4.0 CONCL U S ION

Characterization of Cu film that was subjected to various post-seed self-annealing duration indicated that the Rs of Cu film dropped significantly for the samples that were subjected to self-annealing time up to six hours. Beyond six hours of post-seed self-annealing, the Rs stabilized. The drop in Rs was accompanied by a reduction in Cu film stress which attributed to the grain growth of the Cu film. This indicates that there is an opportunity for the 12 hours maximum delay time between seeding and ECP process to be extended up to 36 hours or beyond to give more flexibility in production scheduling.

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REFERENCES

- [1] F. Wei, L. Li and L. Liu, "Facile synthesis of copper nanostructures through simple replacement reaction," in 10th IEEE International Conference on Nano/Micro Engineered and Molecular Systems, Xi'an, China, 2015, pp. 160-163.
- [2] J.W. Lim, Y. Ishikawa, K. Miyake, M. Yamashita and M. Isshiki, "Influence of substrate bias voltage on the properties of cu thin films by sputter type ion beam deposition", *The Japan Institute of Metals. Materials Transactions*, vol. 43, no. 6, pp. 1403-1408, 2002.
- [3] R. W. Vook, "Electrical control of surface electromigration damage", *Thin Solid Films*, vol. 305, no. 1-2, pp. 286-291, 1997.
- [4] L. Pryor, R. Schlobohm and B. Brownell. (2008). A Comparison of Aluminum vs. Copper as Used in Electrical Equipment [Online].
 Available: http://apps.geindustrial.com/publibrary/checkout/Alum-Copper?TNR=White%20Papers%7CAlum-Copper%7Cgeneric
- [5] D. Edelstein, C. Uzoh, C. Cabral, P. DeHaven, P. Buchwalter, A. Simon, E. Cooney, S. Malhotra, D. Klaus, H. Rathore, B. Agarwala and D. Nguyen, "A high-performance liner for copper damascene interconnects," in IEEE 2001 International Interconnect Technology Conference, Burlingame, California, 2001, pp. 9-11.
- [6] K. Pantleon and M. A. J. Somers, "In situ investigation of the microstructure evolution in nanocrystalline copper electrodeposits at room temperature", *Journal of Applied Physics*, vol. 100, no. 11, pp. 114319-114326, 2006.
- [7] W. Wu, D. Ernur, S.H. Brongersma, M. Van Hove, and K. Maex, "Grain growth in copper interconnect lines", *Microelectronic Engineering*, vol. 76, no. 1–4, pp. 190–194, 2004.

- [8] R. Huang, W. Robl, H. Ceric, T. Detzel and G. Dehm, "Stress, sheet resistance, and microstructure evolution of electroplated cu films during self-annealing", *IEEE Transaction on Device and Materials Reliability*, vol. 10, no. 1, pp. 47-54, 2010.
- [9] S. P. Hau-Riege and C. V. Thompson, "In situ transmission electron microscope studies of the kinetics of abnormal grain growth in electroplated copper films", *Applied Physics Letters*, vol. 76, no. 3, pp. 309–311, 2000.
- [10] J. M. E. Harper, C. Cabral Jr., P. C. Andricacos, L. Gignac, I. C. Noyan, K. P. Rodbell and C. K. Hu, "Mechanisms for microstructure evolution in electroplated copper thin films near room temperature", *Journal of Applied Physics*, vol. 86, no. 5, pp. 2516-2525, 1999.
- [11] B.A. Tik Sun, "Classical size effect in copper thin film: Impact of surface and grain boundary scattering on resistivity," Ph.D. dissertation, Department of Mechanical, Materials, and Aerospace Engineering, University of Central Florida, Orlando, Florida, 2005.
- [12] G. Brunoldi, S. Guerrieri, S.G. Alberici, E. Ravizza, G. Tallarida, C. Wiemer and T. Marangon, "Self-annealing and aging effect characterization on copper seed thin films", *Microelectronic Engineering*, vol. 82, no. 3-4, pp. 289–295, 2005.
- [13] S. Lagrange, H. Brongersma, M. Judelewicz, A. Saerens, I. Vervoort, E. Richard, R. Palmans and K. Maex, "Self-annealing characterization of electroplated copper films", *Microelectronic Engineering*, vol. 50, no. 1, pp. 449–457, 2000.
- [14] W. H. Teh, L. T. Koh, S. M. Chen, J. Xie, C. Y. Li and P. D. Foo, "Study of microstructure and resistivity evolution for electroplated copper films at near-room temperature", *Microelectronics Journal*, vol. 32, no. 7, pp. 579–585, 2001.