EXPERIMENTAL STUDY ON CHEMICAL MECHANICAL PLANARIZATION PROCESS BY MANUFACTURING AUTOMATED SYSTEM

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ABSTRACT: Chemical Mechanical Planarization (CMP) process is one of the critical processes in semiconductor manufacturing. Since in typical semiconductor fab running with high volume and mixed products, good CMP process is required. The process is about planarization. In order to achieve a uniform planar surface, the process control is applied through Integrated Metrology or in this case it is Integrated Thickness Monitoring (ITM) system. ITM simplifies the process control by integrating process and measurement activities in one step. ITM provides feedback on wafer to wafer processing through metrology equipment co-existence in the process equipment. Nevertheless, there is limitation to integrated metrology features, such as recipe matching on individual equipment. In manufacturing facilities, alternative is required to overcome this. Hence, manufacturing automated system capability is extended through Computer Integrated Manufacturing (CIM) system as an alternative to the ITM system, which is called Automated Planarization System (APS). The effectiveness of the alternative system is validated through an experiment. Experiment is done with APS and ITM setup to process similar quantity of wafers. The objective is to observe the process output between the two setups.

KEYWORDS: *Chemical Mechanical Planarization; Integrated Metrology System; Manufacturing Execution System; Automated Planarization*

1.0 INTRODUCTION

There are hundreds of steps involved in a semiconductor manufacturing. The facility is also known as wafer fab. The process steps as well as measurement steps are applied to convert a bare silicon wafer to wafer with millions of transistors circuits. Few wafers are slotted together in a carrier and the combination of both is called a lot. The processes involved are for instance Physical or Chemical Vapor Deposition (PVD, CVD), Chemical-Mechanical Planarization (CMP), Plasma Etch, Rapid Thermal Processing (RPT) and photolithography [1]. The integrated circuits (IC) produced are small in scale and becoming smaller as the technology advances.

Semiconductor industry requires high capital cost compared to other manufacturing industries. Hence, this demands manufacturers to maximize equipment utilization in order to avoid idling time and down time. In addition, technology advancements mean the mix of product changes constantly. New products are continually introduced and old ones are phased-out [2].

The process is becoming complex and demanding. Therefore, process control is critical in each of the processes. At post process steps, control operations are applied at different levels such as product, process and equipment for verification that the process is still under control and the product is still within specifications [3]. In wafer fabrication, thin layers of electrical conductors, semiconductors and insulators are deposited. Then, there are slotted in with implant, anneal, etch or planarization on the surface. Figure 1 illustrates the position of CMP in between of deposition and photolithography.

This article focuses on the integration of process control at CMP with human, who is the manufacturing operator (MO) and the equipment. The integration is made possible with the Computer Integrated Manufacturing (CIM) system. Process control proposed is with Statistical Process Control (SPC) and Engineering Process Control (EPC) to provide control limit on the particular parameter as well as to provide optimum process parameter at processing step. Then, with the system setup, experiment is done at CMP process to validate the effectiveness of the process control.

2.0 LITERATURE REVIEW

2.1 CMP Process

CMP process is an enabling step at interconnect layer on the integrated circuit. As the nodes size shrinking, the planarization process becomes stricter due to requirements on thickness, spatial uniformity, planarity, thermal stability and mechanical integrity [1]. Wafer surface becomes uneven as a result of multiple oxide and metal layers deposited onto the etched surface. CMP is applied to produce a planar mirror-like wafer surface by even off macroscopically flat wafer to atomic level.

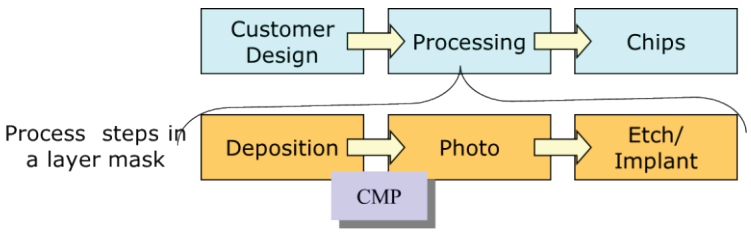

Figure 1: CMP position in a process flow

2.2 CMP Components

CMP process is a synergy of chemical and mechanical applications. A mechanical part of CMP process is about rotating wafers and polishing pads, while a chemical part is on outflow slurry containing chemical reagents and abrasive particles [3-5]. The main components and their functionality are:

i. Platen: A rotating base that fixed the component placed on top.
ii. Pad: An abrasive pad covering and rotating with the platen. This would polish the surface of the wafer.
iii. Carrier: A set of retaining ring, backing film, carrier housing and back press vacuum.
iv. The retaining ring on a backing film holds the wafer upside down as well as keeps the wafer in horizontal position for level polishing.

Carrier that holds the wafer are then counter rotated, meanwhile slurry comprising both abrasives and reactive chemicals is let to outflow. Material is removed through force rotation of polishing pad and wafer. This is strengthened by liquid slurry. In addition, the

rotational speed of carrier and platen are varied [6]. Figure 2 depicts the basic components of CMP.

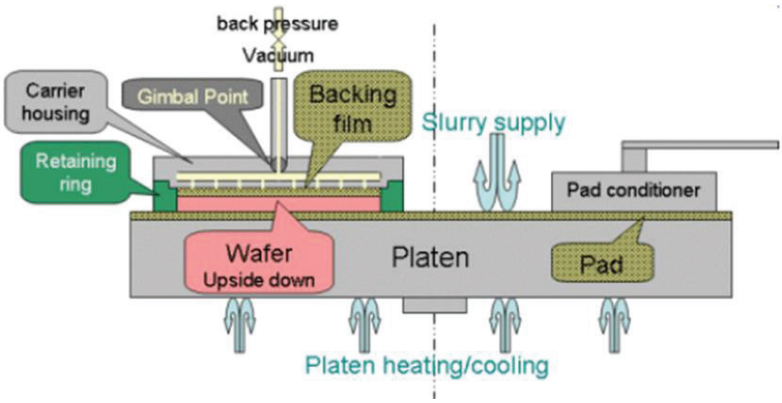

Figure 2: Basic components in CMP process

The process goal is to obtain uniform wafer with a specified target thickness after the polish operation. By virtue of pad and wafer movement, a uniform removal across the wafer is achieved. The challenge is to control the average post-polish thickness in a high volume production with a consistently changing product mix. There are three main sources of variation in post-polish thickness; incoming thickness variation, different pattern density on device layer combinations and drifting in polish rate [7-11].

3.0 METROLOGY MODULE

Integration of metrology in the main process control has been critical development in semiconductor. Integrated Metrology (IM) has been defined as measurements or process control using sensors either inside the process chamber or part of a cluster equipment. Meanwhile, offline metrology or ex-situ measurement is not integrated and may be located close or away from the processing machine. There are discussions on colder approach from manufacturers to switch to IM because of measurement capability and precision of most integrated tools are lacking the performance of leading offline tools, integrating a metrology module in a cluster process equipment, such as lithography, might cause less throughput of the process equipment and the reliability of metrology module might directly impact on process equipment reliability [9,12].

These are a few examples on process running with ex-situ measurement. In Diffusion batch process, Low Pressure Chemical Vapor Deposition (LPVCD) and Atomic Layer Deposition (ALD) nitride processes are dealing with temperature. In addition, as the process involves 5 lots or 125 wafers ideally, nitride deposition and wafer surface characteristics are critical. Monitoring is done through recipe settings and previous run data. After measurement, the post process metrology data would be stored. Then, the data is reapplied to the next run [13]. Then there are critical measurements, which is called critical dimensions (CDs) and are applied at lithography and etch. CD is defining the electrical performance on transistors or interconnects. The main equipment that measuring the transistor gates length is scanning electron microscope (SEM). It is an offline or ex-situ measurement using dedicated equipment and able to produce relatively accurate measurements [7]. Meanwhile, the other example of processes is chemical vapor deposition (CVD) that is to deposit thin films onto silicon wafer substrates. For monitoring, thermocouple readings from CVD chamber on equipment can be used directly for monitoring [8,14]. Besides, there is plasma etch process. It is a highly complex process that makes etch variable measurement very intricate. The attempts to perform in-situ measurement can disturb etch process. Hence, optical and electrical measurements of the wafer are done later at metrology equipment [15].

CMP is the area where IM has been adopted since the similar optical film thickness metrology unit can be integrated with the polisher. There may be complications with the metrology integration, nonetheless the fundamental risk is still at minimum [12]. In CMP, run-to-run process control experiment using IM at factory level has been done previously. In this process control mode, initially a few wafers were processed in the polisher. Then, these wafers were measured and finally the remaining wafers would be processed as well. Thickness data, goodness-of-fit and actual polish time data from the tool was stored and plotted on factory-level process control charts. The charts are to stop equipment from continues processing in out-of-control manner and to alert process engineer [4].

3.1 CMP Process Control

In order to achieve even and planar surface at the first time is a challenge. Re-polishing is necessary for few of the wafers or probably all the wafers in a lot. Therefore, CMP process control is about getting the right removal rate and producing the planar surface. As mentioned earlier, monitoring is required to ensure the success of the process. The process success rate is monitored by measurement either ex-situ or by Integrated Thickness Monitoring (ITM). Ex-situ is measured outside of the process equipment and involving other standalone metrology equipment. Meanwhile, ITM is a software fixed within the process equipment and this allows wafer to be monitored immediately after process completed. ITM carries out measurement in parallel to processing next wafer and the next wafer polishing time is adjusted according to ITM validation. This ensure quick feedback in a process. In this facility, CMP process depends on ITM feature. It simplifies Manufacturing Operator (MO) job and requires minimum intervention from MO.

However, there is limitation to ITM. ITM could be down and as such this impacts process cycle time. MO needs an option to process the wafers even without ITM. Besides, ITM is also required recipe setup for every single new product introduced in the fab, recipe is varied between equipment and it demands equipment time for recipe setup. This is impacting cycle time as well. With this in mind, a comprehensive system is required to imitate the function of ITM. The integration with CIM system is required as it is one of the critical system in a fab and to be applied through ex-situ measurement [2].

4.0 METHODOLOGY

4.1 Integration of CIM and APS Systems

CIM systems play important role in providing automation in a fab. CIM consists of number of components that works together allowing fab running in remote. The two main components in CIM system allowing interaction between MO and equipment are Manufacturing Execution System (MES), Business Rules (BR) and Equipment Interface (EI). There are standard operating procedures (SOP) for MO to run lot on the equipment in automated mode. Series of sequence are:

i. MO placed the lot on the equipment.
ii. Validation is initiated.
iii. Once checking is passed, lot would be processed in the equipment.
iv. Once process completed, MO removed the lot.
v. Lot moved on to the next process and equipment is ready for next lot.

The illustration is shown in Figure 3. This is the routine activities for MO to process and measure the lot as required. This is one of the main criteria on designing Automated Planarization System (APS) to ensure MO routines are uninterrupted and to simplify MO's job [2]. MO is human, while the others MES, BR and EI are software. BR and EI algorithms are enhanced to meet the APS functionality. BR handles the algorithm at process and measurement steps, while EI is at process step. At process step, EI is able to convey the information to actual process equipment, in this case the polishing time. The polishing time is applied by the equipment that is coming from the BR algorithms. Table 1 shows roles of BR and EI in the APS system.

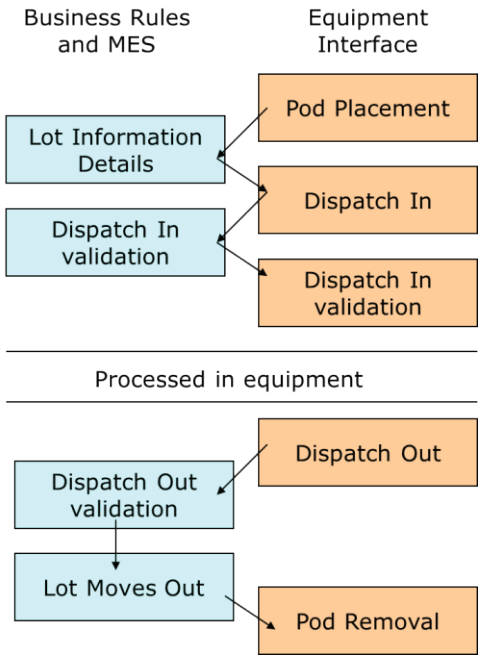

Figure 3: Sequence of activities between Business Rules

Table 1: Business Rules and Equipment Interface functionality

At Measurement Equipment	At Process Equipment
BR: • Store measurement data and wafers information	BR: • Calculate polishing time for each head • Pass the polishing time and the respective head
EI: • Collect measurement data and send to BR	EI: • Apply head information and polishing time on the equipment

In process control, EPC uses measurements to look for changes and adjust the process inputs intended to bring the process outputs closer to targets. EPC is well known in continuous process industries. Meanwhile, SPC uses measurements to monitor a process and look for major changes in order to eliminate the root causes of the changes. SPC is popular in the manufacturing of discrete parts industries for process improvement, process parameter estimation and process capability determination. The integration of EPC and SPC techniques apply an EPC control rule to regulate the system and superimposes SPC charts on EPC controlled system to detect process drifting [14].

In addition, integration of SPC and EPC are applied in the APS. SPC is to check against process control limit by Shewhart chart. Meanwhile, EPC is applied to counterbalance the process by adjusting the variable, in this case the polishing time to produce targeted thickness [5]. Send ahead (SAH) wafers concept is applied whereby a few wafers are sent for process initially, only then run the remaining. SPC is implemented at measurement steps to validate the thickness, either at incoming, post SAH1 and post SAH2. Then, the validation is further implemented at process steps SAH1, SAH2 and Final Commit as shown in Figure 4.

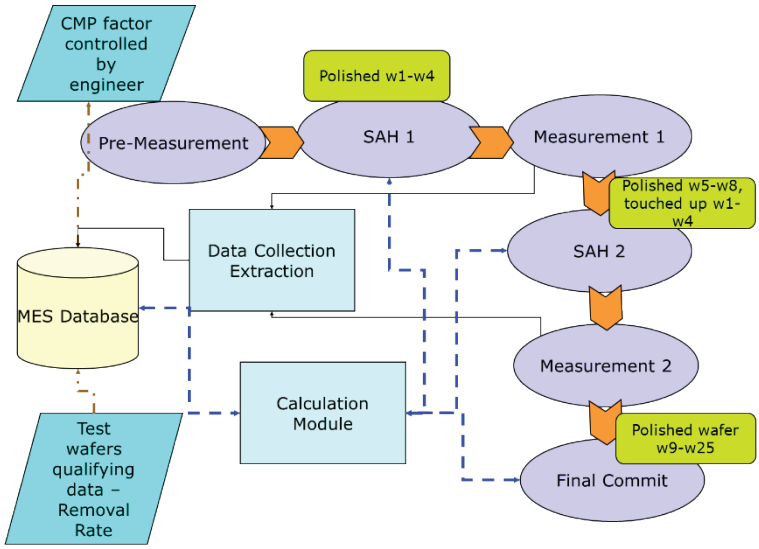

Figure 4: Sequence of activities in Automated Planarization System

4.2 Proposed System Flow

The experiment is focusing on one of the layers in CMP. The APS and ITM models were setup and the main idea was to retain MO standard operating procedures as well as to minimize the changes to MO daily routine. The sequence of activities in APS is shown in Figure 4. Additionally, sequence of activities in ITM is shown in Figure 5. The chemical and mechanical parameters are remaining constant and only the polishing time is varied.

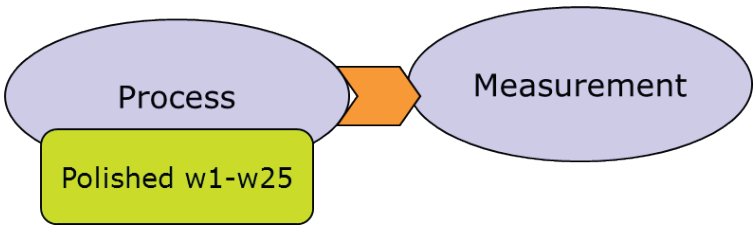

Figure 5: Sequence of activities with Integrated Thickness Monitoring

The experimental setup is done with two different conditions, which are the ITM and the APS systems. ITM system is the current process flow. In ITM, only one process step is required and once it is completed, only then sample wafers would be measured. ITM lot was running at eqp01. Meanwhile in APS as the new process flow, there

are two process steps. The steps are to handle the first process stage of 1-4 wafers at SAH 1 and the second process stage on the remaining wafers at Final Commit, which can be 25 wafers maximum. SAH 2 is available to cater for under polished case during first process stage. Wafers are to be compensate with extra polishing time as well as additional four wafers to minimize cycle time. 5-8 wafers are processed during this time with the optimum polishing time, coming from first process stage and extra time. Measurement is done after each step to validate the thickness data. The first process stage polishes the first 4 wafers as the equipment has four platens to polish wafers at a time. APS lot was running at eqp02.

Experiment was done on 2 lots, 25 wafers each running at two similar equipment settings. Meanwhile, measurement was done on the same equipment, namely as eqpmeas01. Measurement was done on four wafers each, either at ITM or APS lot. The four wafers were randomly picked and thickness data was observed. Only four wafers were selected for sampling purpose as well as representing total number of platens.

5.0 RESULTS AND DISCUSSION

Each lot processed at eqp01 and eqp02 was measured to validate the thickness. Four wafers were selected to represent the four platens performance and also representing the removal rate. Thickness data was obtained from eqpmeas01. Each wafer thickness was measured on number of n sites and controlled by thickness spec limit. Thickness data is considered good if the data point is within the spec limit. The four wafers thickness data were within the spec limit, either running through eqp01 for ITM lot or through eqp02 for APS lot. Two types of observations were made at wafer-to-wafer thickness distributions as well as thickness data variations.

Wafer-to-wafer thickness data distribution is showing as consistent on APS lot compared to ITM lot. The thickness on APS lot shows better average between each wafers, while ITM lot slightly drifted. This can be seen from Figure 6. Meanwhile, on thickness data variations between the two lots, APS lot shows more controlled variations. The thickness data variation is shown in Figure 7. The experiment done with the APS produced comparable results compared to ITM

Besides achieving number of wafers polished, observation is also made on the success rate of the polishing. If APS model able to run the first four wafers successfully, without the need of re-polished, this means the similar polishing time can be applied to the remaining wafers. Better cycle time is achieved as additional step is not required to re-polish the first stage wafers.

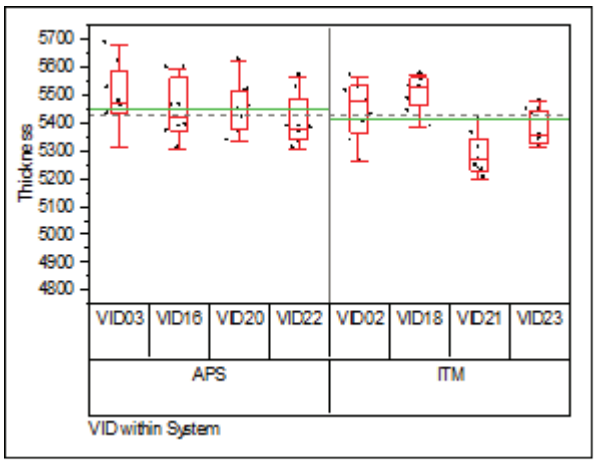

Figure 6: Wafer-to-wafer thickness data distribution

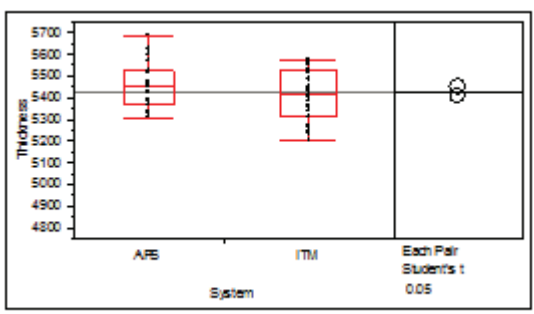

Figure 7: Thickness data variation

6.0 CONCLUSIONS

As CMP is critical as the other process in semiconductor manufacturing, there are various methods applied by the engineer to obtain the optimum polishing time. The wafer surface characteristic is differed from one lot to another. The existing ITM has its advantages and disadvantages. As the economic reason became one of the main disadvantages, engineer is challenged to find way to obtain the ideal polishing time. ITM system able to provide real time measurement and to perform auto-correction for the subsequent lot, but there lies a challenge in mixed products environment. APS is proposed as an alternative to the ITM system.

Engineer has better control on the process as the process and the metrology parts are separated into two different steps. Besides the initial polishing time could be apply to the first few wafers to minimize the impacts to the whole lot. In addition, the first process stage or SAH 1 can be used as benchmark time for the remaining wafers. This eventually would save the process cycle time. Besides, with proper planning APS can reduce cycle time and more importantly avoid MO from running the lot without proper control, which is in local mode and exposed to mistakes.

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