REMOTE GLOBAL ALIGNMENT ERROR FOR CYCLE TIME IMPROVEMENT OF PAD INDUCTOR LAYER

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ABSTRACT: Lithography is the key process which transfers the pattern from mask to wafer and pad inductor layer is the last layer in photo masking. The cycle time for pad inductor layer increase in Silterra Malaysia by 32% of Global Alignment error per month. This induce success rate goes down as low as 50% for pad inductor layer. Long engineering time is taken during troubleshooting of the lot for expose and developing step by manually due to tool time constrain. Most of the lots undergo rework processes which results the cost per wafer to increase. The aim of this research is to reduce the cycle time for pad inductor layers by introducing the "Remote Global Alignment Error" (RGAE) method with alternative flow. This would avoid the pad inductor layers to be sent for rework if it encountered any global alignment error. The experimental result shows RGAE method able to reduce cycle time for pad inductor layer by 97%. This is due to when global alignment error occurs the lot will automatically track in RGAE method by selecting the rejected wafers for expose and developing process. This has eventually saved more time for split wafers which usually send for rework.

KEYWORDS: *Lithography; Pad Inductor; Cycle Time; Rework; Global Alignment*

1.0 INTRODUCTION

Photolithography is a process used in semiconductor device fabrication to transfer a pattern from a photo mask (also called reticle) to the surface of a wafer or substrate. Photolithography, lithography or microlithography is the art and science of printing the circuit element patterns used for the construction of semiconductor devices.

These patterns are replicas of master pattern on a durable photomask, typically made of a thin patterned layer of chromium on a transparent glass. Patterns are first transferred to a photoresist layer.

The photoresist is a liquid film that can be spread out onto a substrate, exposed with a desired pattern and developed into a selectively placed layer for subsequent processing. Advanced lithographic techniques have become important in the field of modern electronics. Such techniques, which include optical (g-line, I-line, Duv), X-ray and electron-beam lithography are used in the microfabrication of integrated circuits and other semiconductor devices.

Alignment is the process of determining the position, orientation and distortion of the patterns already on the wafer and placing them in the correct relation to the projected image [1]. Automatic alignment is a system optically scan the wafer and reticle alignment marks and using either image or signal processing automatically position the two to a high degree of exposure and overlay accuracy. Alignment steps include:

a. Reticle aligns to reticle stage and fiducial mark on the wafer stage.
b. Wafer global alignment to find wafer center relative to wafer stage origin.
c. Enhanced Global Alignment (fine alignment) before exposure.

Since many layers make up a completed wafer, each additional layer must be aligned precisely and accurately with the previous one. Critical dimensions may be less than one micron which places a great burden on the alignment process. Alignment is done with patterns

placed in the scribe lines during the resist development [2]. When subsequent layers are put down, the layer patterns are aligned by adjusting the position of the projection with the alignment marks on the wafer.

2.0 LITERATURE REVIEW

Semiconductor production is a very demanding process. The waiting time often exceeds the processing time. In this scenario, lots have to wait in a queue before any available photolithography tools to process them [3]. Cycle time is an important element in photolithography that gives the same impact in semiconductor manufacturing [4]. Cycle time is the time it takes for a product to be processed, plus the time spent waiting to be processed.

Price for the newest generation of ASML tools which starts at 30 million Euro and the idle time is not economical in photolithography as the idle time is classified as a waste of capital [5]. Industrial studies have shown that on average by reducing the cycle time by one percent will decrease the cost per produced wafer by 0.7 percent [6]. The photolithography cycle time is about 10% of the total cycle time [4].

Misalignments such as translation, rotation and expansion misalignment have been studied in lithography in the form of mask to wafer alignment and in the form of the wafer to wafer alignment [7-8].

Those days, wafer-to-wafer alignment technique only used for MEMS process. It was developed specially for aligning the wafers in MEMS process [9]. However, today this technique is the most important technique in manufacturing photolithography semiconductor [10-11]. It is because wafer-to-wafer alignment technique mostly used for metal-to-metal bonding technology in MEMS application [12-13].

All the semiconductor company will try to reduce the cycle time. This is due to increased throughput (WPH). By reducing the cycle time, the company can reduce operating and inventory costs, can increase the quality and able to be competitive to respond fast to meet customer's need [14-15].

3.0 METHODOLOGY

3.1 Current Method

The current method that uses C18 technologies for pad inductor layers has many issues during the production. These issues include:

i. High wafer rejects rate due to global alignment error.
ii. High cycle time due to the rejected wafers.
iii. High rework rate
iv. High cost consumption

From all these issues, the main issue is global alignment error during align the wafer with a scanner. Due to some parameters that explain previously not meet, the wafer will be rejected. There are 2 options to process the rejected wafers include:-

a. Manually expose and develop the reject wafers
b. Rework the rejected wafers

When the production lot track in at the litho cell (Coat-Expose-Develop), the first step is to coat the wafers at track tool. All wafers will be coated; then the wafers will be sent to the scanner for exposing. Before the exposing process, the wafer will be aligned one by one using a particular alignment mark. A wafer will reject from the stepper during a run if it fails to successfully align.

On the other hand, when alignment methods or marks are changed, the occurrence of rejects is followed closely. Then, the process engineer needs to get permission from the manufacturing department for manual processing. Moreover, the process engineers need to select the track recipe and scanner job by manually for processing the lot. If the process engineer wrongly selected any recipe at track tool can cause the wafer has been double coat and send to the scanner. If the scanner successfully exposes the wafer, this wafer will send for the next step and will encounter this wafer will be scrapped.

Most of the time, the manual job that was done by process engineers for aligning the wafer that still encounters a global alignment error; as last chance the wafers will hold for the split and send for rework.

Normally, on average two to three hours are needed due to pod constrain for splitting the wafers and send for rework. Average six to eight hours needed for reworking the wafers. After rework process, the reject wafers will use less loosen of setting for aligning the wafers. If still a reject the wafers and then we need repeat again all process that explains earlier. This will take eight to ten hours to complete all the processes.

3.2 Proposal Method - Remote Global Alignment Error (RGAE) Method

The current method encounters many issues and induces cost per wafer increases. After collecting all the data and analyze the data from the current method, this research propose a new method called "Remote Global Alignment Error" (RGAE) method. Figure 1 shows those proposed RGAE methods that reduce cycle time for pad inductor global alignment error due to rejecting wafers will run again automatically until the wafers successfully expose.

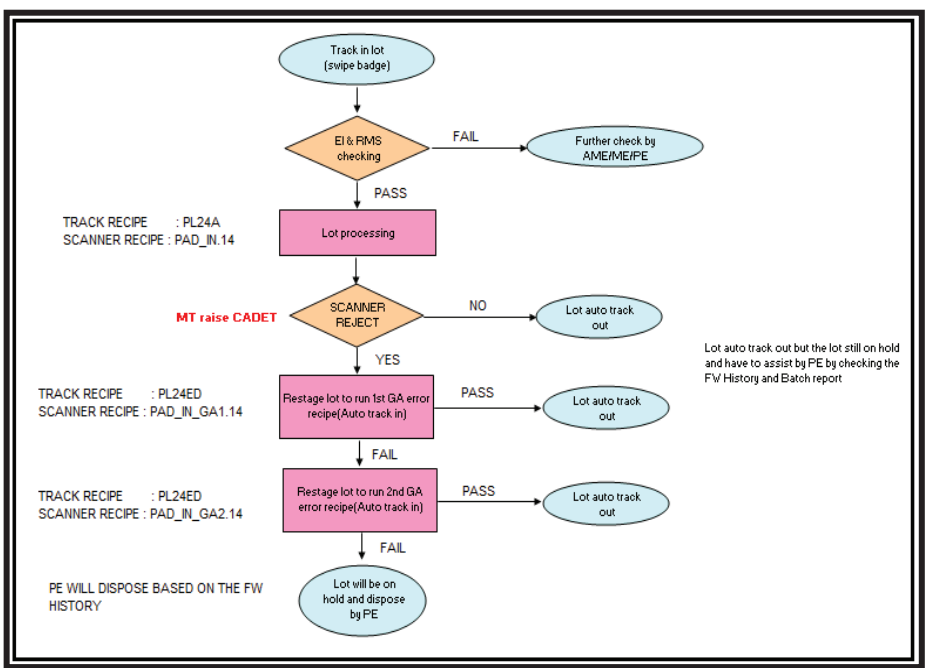

Figure 1: RGAE method

This paper evaluates the alternative flow for reducing cycle time for Pad Inductor Layer. The new process flow identified as Remote Global Alignment Error (RGAE) method. The features of RGAE's method as per below:-

i. Only can use for C18 technology devices that have Pad Inductor layer only. The script already hard code to avoid the use of other technology or devices.
ii. Every device that has pad inductor layer will only use one track recipe, namely "PL24A". After that, when encounter global alignment error, the system automatically loads RGAE flow method. Then, only "PL24ED" track recipe that can use in RGAE method. Another track recipe does not allow for RGAE method.
iii. Moreover, every device that has pad inductor layer will only use one scanner job file, namely "PAD_IN.14". After that, need advance create the new scanner job file name "PAD_IN_GA1.14" for 1st time global alignment error reject wafers. Consequently "PAD_IN_GA2.14" need advance create for 2nd time global alignment error reject wafers. Another scanner recipe does not allow for RGAE method. All scanner job files need to create at ASML server.
iv. Does not have "send ahead" step. This is due to RGAE method already designs to use in a floating system in meanwhile "send ahead" step also one of the floating systems. Moreover, in one system cannot have two floating system that can make the system hang.
v. Does not have rework flow. Once production lot track in at track tool and if encounter global alignment error, the system automatically load flow for RGAE method. In this new flow, the rework flows never design in this RGAE floating system. This is because to avoid accidentally the lot send for rework while the lot encounter global alignment error.
vi. In RGAE method, the flow is design for a looping system. This is for avoiding the effect on daily tool throughput. Therefore the looping system at GA_PADIND path step only allows 3 times only.

vii. After 3 times, if still encounter global alignment error; all the rejected wafers need to split at Visual Inspection step. Then after the split, the lot need send for rework.
viii. All global alignment error rejected wafers need create "Cadet" for the documented purpose. This is for traceability for future analysis for verify how many wafers encounter global alignment error and to calculate the success rate RGAE method.
ix. The RGAE method needs special privilege for skip global alignment step (GAStep) that will allow for Global Alignment path only. This mean, not all engineers or technician can have the privilege to run RGAE method.
x. After running all rejected wafers due to global alignment error using RGAE method; the process engineer or technician should be to place future holds at Visual Inspection step for 100% visual inspection for verify the wafers encounter misalignment or any abnormal on the wafers.

Table 1: Summary of the difference between current method vs RGAE method

No	Process	Current Method	RGAE Method
1	System	Manual	Remote
2	Rework	High	Low
3	Manpower	Only Process Engineer	All
4	Cycle Time	High	Low
5	Traceability	No	Yes
6	Cost per Wafer	Expensive	Cheap
7	Human Error	High	No

4.0 RESULTS

The experiments results presented here in order to evaluate the performance of Remote Global Alignment Error (RGAE) Method compare to the current method. The purpose of experiment and test result is to make sure achievement of the objective of the research. That's is to develop a system that able run automatically the rejected wafers due to global alignment error to reduce cycle time for C18 technology devices of Pad Inductor Layer.

4.1 Two-Sample T-Test and Confidence Interval for Cycle Time Between Current and RGAE Method

A hypothesis test for two populations means to determine whether they are significantly different. This procedure uses the null hypothesis that the difference between two population means is equal to a hypothesized value (H_0: $\mu_1 - \mu_2 = \mu_0$)) and tests it against an alternative hypothesis; which can be left-tailed ($\mu_1 - \mu_2 < \mu_0$) right-tailed ($\mu_1 - \mu_2 > \mu_0$) or two-tailed ($\mu_1 - \mu_2 \neq \mu_0$). If the test's p-value is less than chosen significance level; then should reject the null hypothesis.

The first step of a hypothesis test is to determine the null and alternative hypotheses. The null hypothesis usually specifies that a parameter equals a specific value. For this research, the difference in the mean numbers of cycle time for current and new RGAE method equals 0 (H_0: $\mu_{CURRENT} - \mu_{RGAE} = 0$). This is due to, do not suspect beforehand that one method has a greater mean number of complaints than the other; a two-tailed test is appropriate.

Therefore, the hypotheses for the test are:
a. H_0: $\mu_{CURRENT} - \mu_{RGAE} = 0$
b. H_1: $\mu_{CURRENT} - \mu_{RGAE} \neq 0$

The key output from Figure 2 begins at the line 'Difference = ($\mu_{CURRENT} - \mu_{RGAE}$). So the difference is considered as the mean for the current method minus that for the new RGAE method ones and the point estimate for that difference is given on the next line as 1.940. In this case, Minitab's insistence on arranging terms in alphabetical order has led to a happy situation where the calculated difference is positive when cycle time increases as per illustrate in Figure 3.

Two-Sample T-Test and CI: CURRENT, RGAE

Two-sample T for CURRENT vs RGAE

	N	Mean	StDev	SE Mean
CURRENT	65	1.99	4.20	0.52
RGAE	60	0.0476	0.0403	0.0052

Difference = μ (CURRENT) - μ (RGAE)
Estimate for difference: 1.940
95% CI for difference: (0.900, 2.981)
T-Test of difference = 0 (vs ≠): T-Value = 3.73 P-Value = 0.000 DF = 64

Figure 2: T-Test and confidence interval for cycle time between current and RGAE method

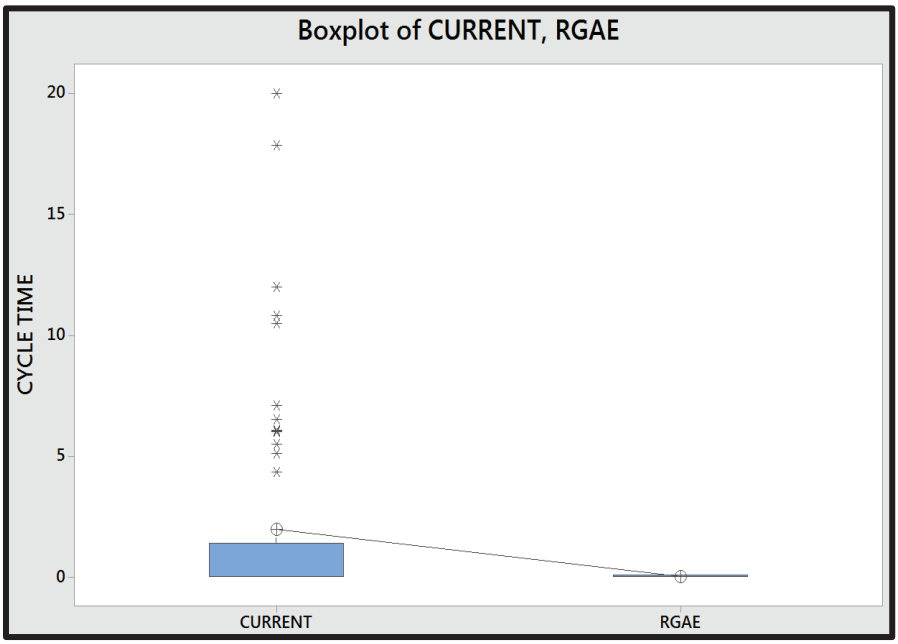

Figure 3: Boxplot base on two-sample t-test and confidence interval

The confidence interval for the difference is based on this estimate and the variability of the samples. This gives a 95% confidence interval for the difference in the means ($\mu_{CURRENT} - \mu_{RGAE}$) as (0.9, 2.981) and calculates the P-value as 0 for the test of H_0: $\mu_{CURRENT} - \mu_{RGAE} = 0$ versus the alternative H_1: $\mu_{CURRENT} - \mu_{RGAE} \neq 0$. In this case, the test rejects H_0. The conclusion in this case, is that the means of the two data sets are not equal.

The T-value for the test is 3.73, which is associated with a p-value of 0. Thus, it can reject the null hypothesis at the α = 0.05 level and conclude that there is a statistically significant difference between the mean number of cycle time for current and new RGAE method.

4.2 Comparing Variance Test for Cycle Time between Current and RGAE Method

This research uses the two Variances test to determine whether the variances or the standard deviations of two methods are different. Then, the calculation was made on a range of values that is likely to include the population ratio of the variances or the standard deviations of the two methods (current and RGAE).

On the other hand, the two variances are useful for quality improvement situations for this research. The research can use this test to compare the variance within subgroups to the variance between subgroups. Moreover, the research also can use this test to compare the process variance between current and new RGAE method after implement a quality improvement program.

Figure 4 illustrates two variances test and confidence interval cycle time between current and new RGAE method using F-test. Moreover, Figure 5 illustrates two variances test and confidence interval cycle time between current and new RGAE method using Bonett's and Levene's test.

The results from Figure 4 illustrate that $S_{CURRENT}$ = 4.199 and S_{RGAE} = 0.04. The test statistics *F-test* is computed as $F = S^2_{CURRENT} / S^2_{RGAE}$ = 10878.93. Since $H_0:\sigma^2_1-\sigma^2_2=0$ is equivalent to either $H_0:\sigma^2_1 / \sigma^2_2=1$ or $H_0:\sigma^2_2 / \sigma^2_1=1$. On the other hand, the p-value is 0 and less than the significance level (denoted as α or alpha) of 0.05; the test rejects the null and conclude the two methods (current and RGAE) variances are not significantly equal ($H_0:\sigma^2_1 / \sigma^2_2 \neq 1$).

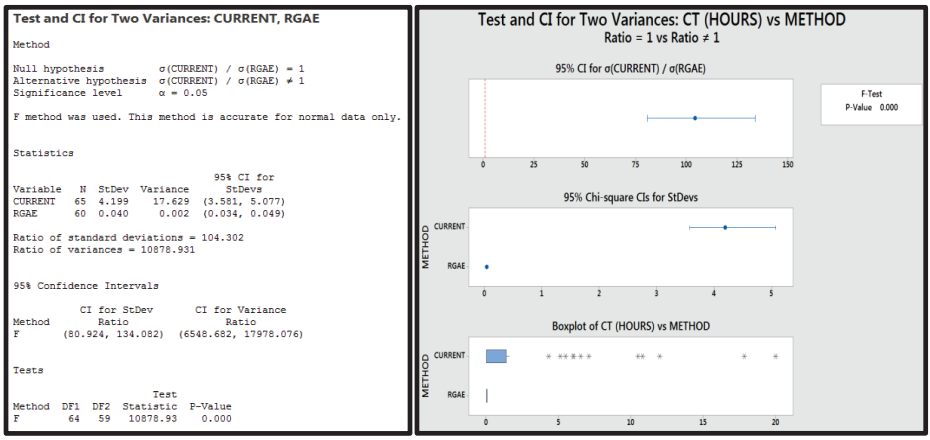

Figure 4: F-test graph for current and RGAE method

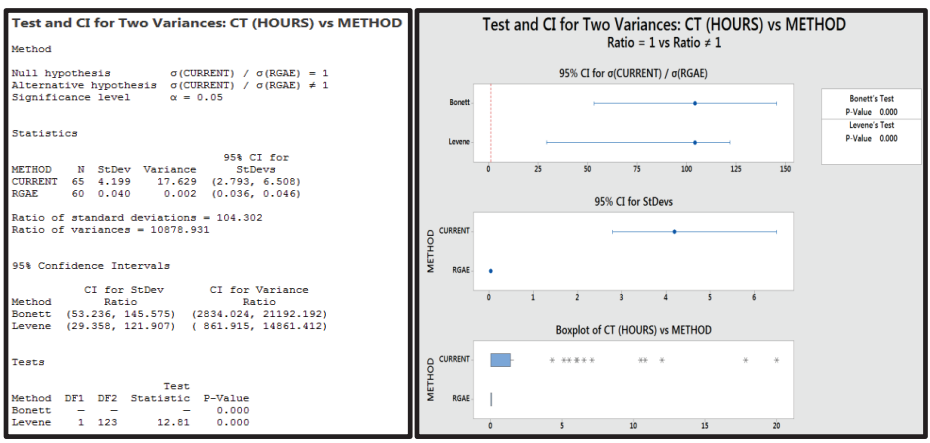

Figure 5: Bonett and Levene test graph for current and RGAE method

The results from Figure 5 illustrate that $S_{CURRENT}$ = 4.199 and S_{RGAE} = 0.04 same result as F-test. The test statistics for Levene's test is computed as 12.81. The null hypothesis states that the ratio of the two methods (current and RGAE) standard deviations is 104.302 and the alternative is that the ratio is 10878.931 are not equal.

Minitab calculates the 95% confidence intervals for the standard deviation and variance ratios. These intervals contain more than 1, then there is enough evidence to suggest that the standard deviations or the variances of the methods are not equal as illustrated in Figure 4 and Figure 5.

The p-values results of Bonett's test and Levene's test as per shown in Figure 5 are 0 and less than the significance level (denoted as α or alpha) of 0.05; the test rejects the null and concludes the two methods (current and RGAE) variances and standard deviations are not significantly equal.

4.3 Cycle Time Comparison between Current and New RGAE Method Using Production Lot

Table 2 and Figure 6 shows the cycle time comparison between the current and RGAE method for a C18 technologies pad inductor layer using real production lot. In this DOE test run, five different devices from C18 technologies were selected and compared the cycle time with current and new RGAE method. The cycle time calculated starts from lot track in, followed by split reject wafers, subsequently exposure again and merge all wafers before moving to next step. There is a maximum of 25 wafers in one lot. In some cases, the quantity of the wafers will be less than 25 wafers due to having some issue on the wafers that could be scrap or split the wafers into child lot. The quantity of the wafer rejected for a current and RGAE method is same.

Table 2: CT comparison between current and RGAE method for pad inductor layer

METHOD	CT_HOUR	TOTAL WAFER	WAFER REJECT
CURRENT	46.25	25	3
CURRENT	23.20	25	4
CURRENT	32.50	24	2
CURRENT	19.40	20	3
CURRENT	25.30	25	5
RGAE	0.55	23	2
RGAE	1.15	25	5
RGAE	1.10	25	5
RGAE	0.55	24	1
RGAE	1.05	25	3

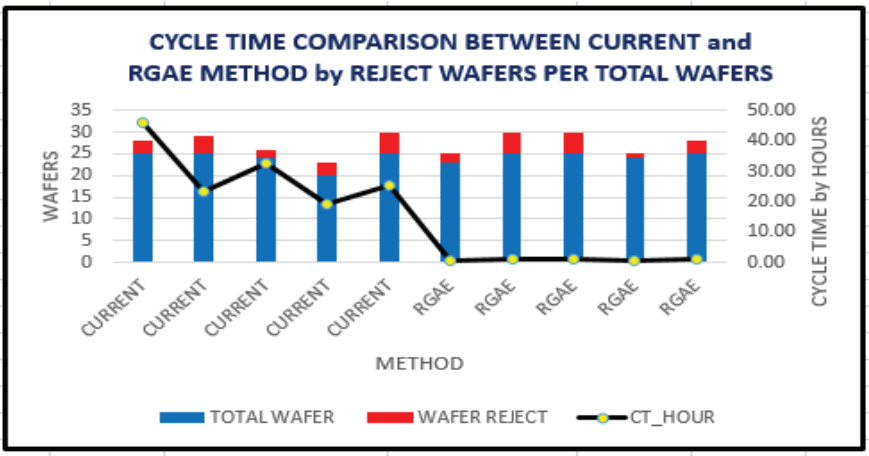

Figure 6: Cycle time comparison between current and RGAE method for pad inductor layer

The cycle time performance for current method increases until almost 46 hours. This is due to the rejected wafers that causing global alignment error needs to split further. Unfortunately, most of the time in Silterra Sdn Bhd encountering high "wip" and shortage of port which causing the manufacturing part taking a long time to split the wafers.

Subsequently, the split wafers go to rework step. During the rework process, ETCH module gives most priority on other important production lots which resulting in less focus on rework lot; again this delayed process on reworking increases cycle time for pad inductor layer. After rework, the split wafers need run again. During the remask process, photolithography module gives priority on other important or urgent production lots rather than run remask lots.

Moreover, the aging or waiting for time increase in cycle time for pad inductor layer. After remask, all the wafers need to merge with parent lot. However, the cycle time for RGAE method achieved within 2 hours. This success could be achieved by allowing the rejected wafers to run automatically by using alternative flow until the wafers successfully expose. By having the new method (RGAE), the production can save time for the split, rework, remask and merge all the wafers.

Figure 7 shows that the total average cycle time improvement achieved by 97% when using this new RGAE method for the C18 technologies pad inductor layer. This chart clearly shows that the five devices that using current method have high cycle time. In contrast, the new RGAE method has less cycle time with less than 2 hours cycle time consequently for five devices. Thus, this shows that the repeatability of the new RGAE method is more stable when releasing to production.

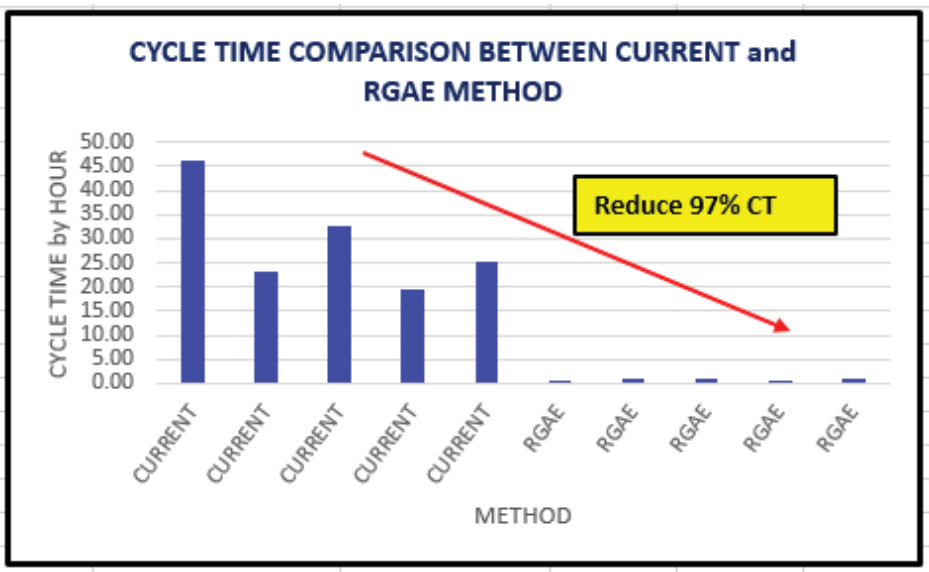

Figure 7: CT reduction on RGAE method compare to current method for pad inductor layer

5.0 CONCLUSION

The goal of this research is to reduce cycle time for pad inductor layer due to global alignment error. This research has two objectives:

a. By introducing the Remote global alignment error (RGAE) method.
b. Introducing alternative flow to avoid split and sending rejected wafers for rework.

Both objectives are successfully implemented and the goal to reduce cycle time for pad inductor layer was achieved. This was verified during the test run with five different devices for the pad inductor

layers which have global alignment errors. All rejected wafers automatically selected and successfully "track in" inside tool using alternative flow that has a different alignment mark. Finally, all rejected wafers were exposed to avoid the split and rework. The average cycle time of 97% improvement can be achieved when switching from current method to new method (RGAE). This achievement reduces significantly cycle time for the pad inductor layer for C18 technologies.

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